FINAL REPORT
FOR
SILICON-BASED OXIDE/SILICON/OXIDE RESONANT TUNNELING

CONTRACT NO. F49620-95-C-0001
1 December 1994 – 31 March 1998

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13. ABSTRACT *(Maximum 200 words)*

We explored two metholds for forming SiO2/Si/SiO2 resonant tunneling diodes with crystal-line silicon quantum wells. The first method, growth through voided oxide, was successful in demonstrating for the first time that crystalline Si can be grown through voids in the oxide. However conditions for forming the small void size needed to block electron transport, while allowing nucleation of silicon through the oxide, were not found. A systematic search of the growth temperature-pressure space showed that these conditions do not come naturally for the (100) and (111) surfaces. For this reason, we adopted a lateral-over-growth approach in the final year to fabricate the RTD.

The SiO2/Si/SiO2 resonant tunneling diodes grown using the lateral silicon overgrowth process did not show the desired negative differential resistance characteristic, but test on these diodes indicate that the desired heterostructure has not yet been achieved This process has now been transferred to DARPA's Si-Based Quantum MOS Technology Development program (Contract No. F49620-96-C-0006), where it will be used for lateral overgrowth of RTD heterostructures.

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I. OBJECTIVES

The objective of this program was to demonstrate resonant tunneling diodes (RTDs) based on the $SiO_x/Si/SiO_x$ double-barrier heterostructure with amorphous oxide barriers but with crystalline silicon (c-Si) quantum well. A schematic band diagram illustrating the target heterostructure is shown in Figure 1. Circuit simulations indicate that such a diode in silicon and integrated with CMOS or bipolar transistors can increase circuit speed by 2 to 10× and reduce static power dissipation in SRAM and DRAM by 100×. The SiO_x/Si system is attractive both because of the demonstrated high quality of the oxide/silicon interface and because RTDs formed with these materials would not require the introduction of new materials into current silicon production facilities. The key technical impediment to successful growth of the SiO_2/Si double-barrier heterostructure is the growth of the single-crystal silicon quantum well on the silicon oxide surface.

We proposed two methods for forming single-crystal, silicon/oxide, double-barrier structures. The first method is based on the formation of oxides with nanometer scale voids and the nucleation of crystalline Si through the voids.[1] The voids in the oxide tunneling barrier have openings of sizes smaller than the electron wave packet spread, to ensure crystal alignment through the diode without diminishing the tunneling barrier height. In the second method, the crystalline Si quantum well is formed over lithographically-defined oxide islands, by molecular beam lateral epitaxial overgrowth. In this case, the greater silicon surface provides the seed for lateral crystalline overgrowth of the oxide islands. These two approaches are illustrated in Figures 2 and 3.

II. ACCOMPLISHMENTS

Raytheon TI Systems (formerly Texas Instruments Defense Systems) and Texas Instruments (TI) established conditions for the growth of ultrathin (~1 nm) silicon oxide tunnel barriers on both Si (100) and Si (111) surfaces. Techniques were developed for the controlled formation of voids in these oxides on both Si (100) and Si (111) surfaces by the thermal desorption of SiO from the oxide in ultrahigh vacuum (UHV). For the first time, the growth of crystalline silicon on voided oxide tunnel barriers was demonstrated. The growth parameter space was also mapped out showing the growth conditions [on both (100) and (111) surfaces] under which polycrystalline, amorphous, and crystalline silicon overgrowth results. We found the growth conditions that result in crystalline Si overgrowth correspond to void sizes exceeding 200 nm^2, whereas 3 to 12 nm^2 is required to negate drift and diffusive transport over tunneling.

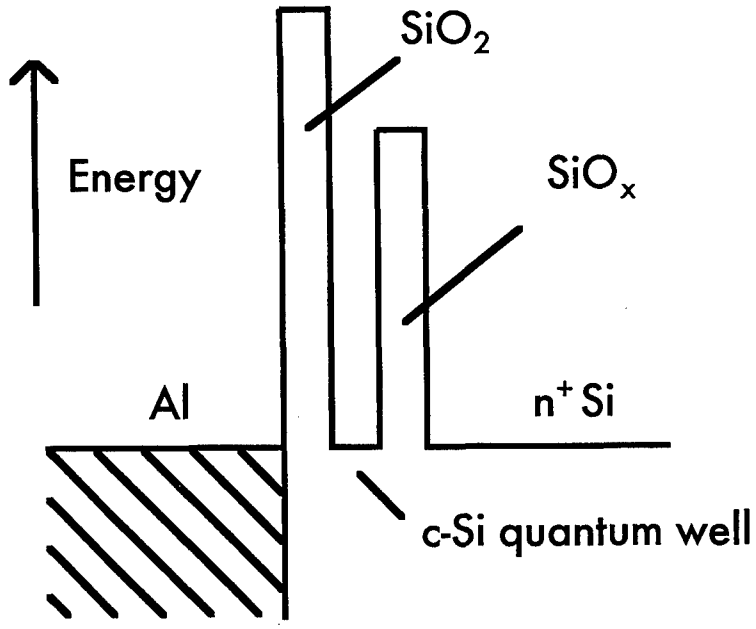

Figure 1. Schematic energy band diagram of a SiO_2/c-Si/SiO_2 resonant tunneling diode with a crystalline Si (c-Si) quantum well.

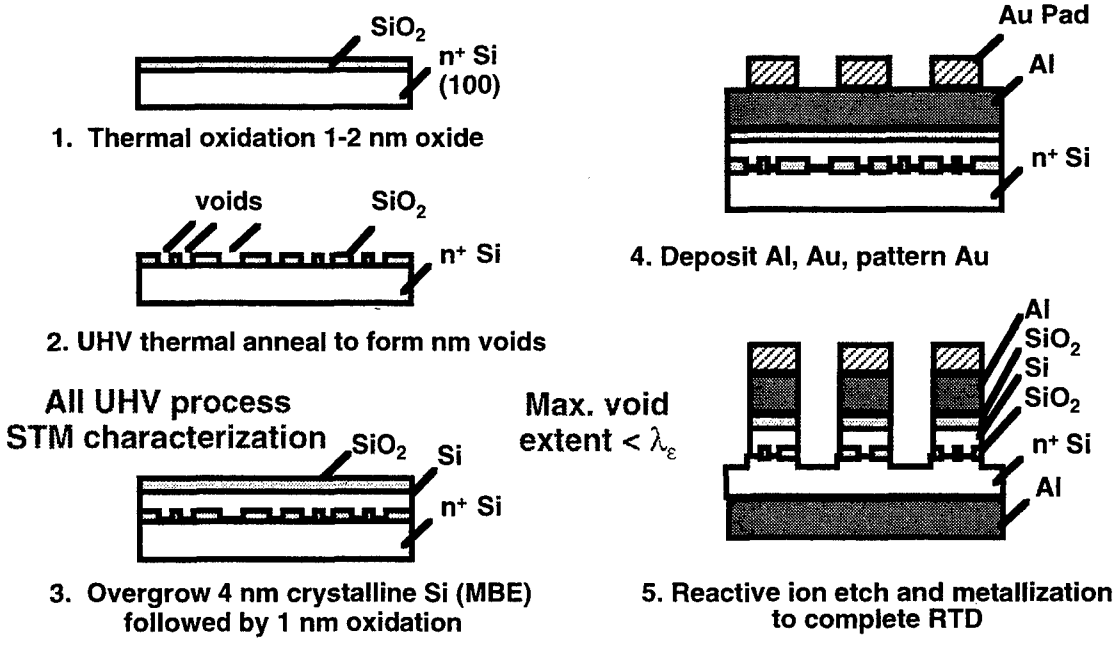

Figure 2. Method for forming SiO_2/c-Si/SiO_2 resonant tunneling diode by formation of oxide voids and nucleation of c-Si through the voids. The oxide voids must have sizes less than the Fermi wavelength (l_e~ 3 nm) to maintain an effective tunneling barrier.

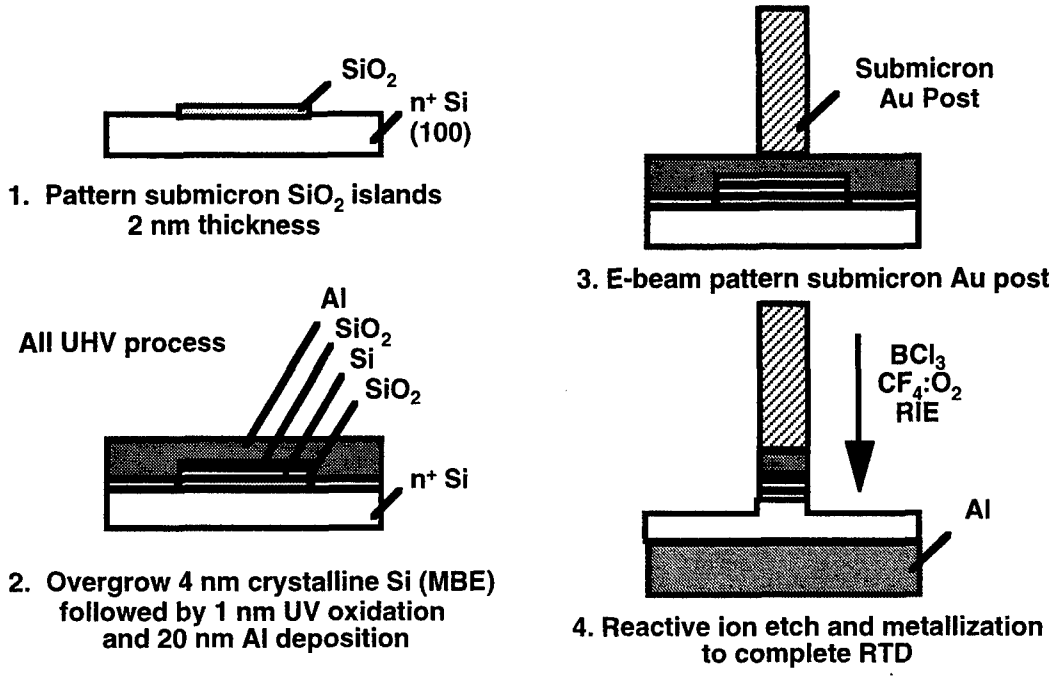

Figure 3. Method for forming SiO_2/c-Si/SiO_2 resonant tunneling diode by lateral overgrowth of c-Si on submicrometer oxide islands.

Double-barrier resonant tunneling diodes were formed on voided oxide and characterized by *in situ* scanning tunneling current-voltage (I-V) measurements and by the *ex situ* formation and measurement of device structures with crystalline, polycrystalline, and amorphous silicon quantum wells. As expected for the large void size that could be obtained from this process, the oxide barrier conducts, and no tunneling resonance in the I-V measurements was observed.

A general finding from the study of voided oxide growth is that, independent of the surface orientation (100) or (111), the void size and density are directly related. As a result, as void size becomes smaller, the spacing between voids becomes larger, which acts against the formation of a continuous crystalline Si overgrown film in favor of polysilicon nucleation on the oxide. For this reason, we decided not to pursue the voided growth further. Instead, in the last year of the program, we focused resources on the lateral overgrowth approach, which now appears to be more promising for producing oxide/silicon/oxide RTDs.

A five-level process and mask set were designed and released for fabricating the SiO_2/Si/SiO_2 RTD. RTDs from this process were grown and characterized, but resonant tunneling was not observed. However, analysis of the measured I-V data indicates that the resonant tunneling was probably suppressed because the thickness of the first tunnel barrier exceeded the design target (~2 nm compared to the target thickness of 1 nm). Because of the large barrier height of the Si/

SiO_2 heterostructure (3.2 eV), resonant tunneling was not expected unless both barriers were approximately 1 nm. The mask and processs have been transferred to the DARPA Quantum MOS Technology program (Contract No. F49620-96-C-0006), where the lateral overgrowth is being optimized.

Band offset calculations were undertaken and completed on a β-crystobalite SiO_2/Si (100) model, where four layers (7.5 Å) of SiO_2 were determined to be necessary to obtain a high conduction band offset. Below this thickness, that band offset is decreased. Further, first-principles calculation of void growth energetics showed that the activation energies for SiO formation and for mobile Si monomer formation on the silicon surface are indistinguishable. If this model is correct, then the result suggests that it is not possible to suppress pin hole (void) formation kinetically in oxides in the temperature-pressure regime examined. While pin holes are desired in the formation of RTDs, they must not be allowed to form in CMOS device processes.

III. FINDINGS

A. Theoretical Limits to Oxide Tunnel Barrier Thickness Determined

A first-principles theoretical study was completed to determine the dependence of the Si/SiO_2 conduction band offset on the thickness of the SiO_2 using a β-crystobalite model for the SiO_2. This calculation, detailed in Appendix A, "Band offset of ultrathin SiO_2-Si (001) interface: a first principles study," was undertaken to provide insight into whether the bulklike behavior of SiO_2 can be expected when the oxides are a nanometer thick or less. The calculation showed that after four layers of SiO_2 (~7.5 Å), the conduction band offset reaches its bulk value of ~3.2 eV.

B. Growth Techniques for Voided Ultrathin Oxides on Silicon (100) Developed

Details of this development are contained in three publications attached as appendices: Appendix B, "*In situ* flux cleaning technique for producing atomically flat Si (100) surfaces at low temperatures"; Appendix C, "Void formation on ultrathin thermal silicon oxide films on Si (100)"; and Appendix D, "Controlled growth of SiO_2 tunnel barrier and crystalline Si quantum wells for Si resonant tunneling diodes." The summary findings for this effort are provided in Figure 4, which presents the dependence of oxide void density and size on annealing time for the (100) surface. For the voided oxide tunnel barrier to work, we need conditions that provide void areas of 3 to 12 square nanometers. Our experiments show that the smallest voids [as determined by scanning tunneling microscopy (STM)] formed by UHV thermal desorption of SiO from ultrathin oxide on Si (100) are ~300 nm^2 (~20 nm diameter). We, therefore, conclude that this technique does not provide a suitable voided oxide for formation of RTDs on the (100) surface.

A first-principles calculation was undertaken to seek other means to control the void formation process. The details of this study are contained in Appendix E, "Energetics of void enlarge-

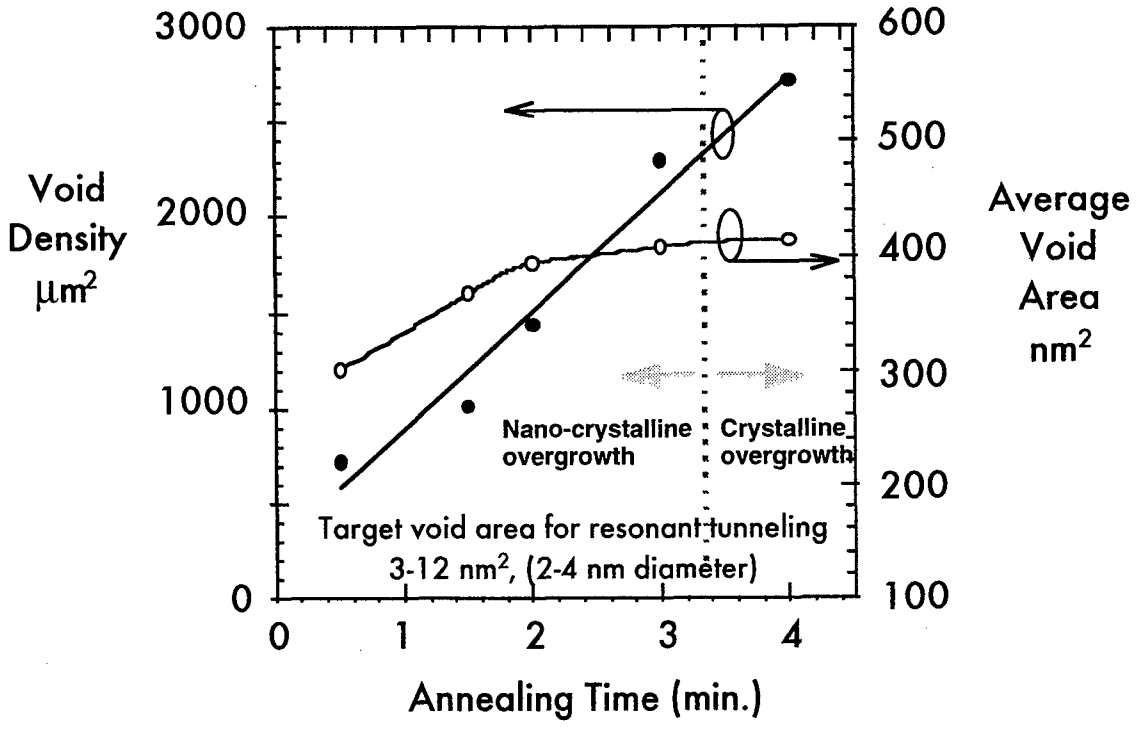

Figure 4. Dependence of the SiO_2 void density and size on the annealing duration. The thermal oxide thickness was 1 nm, grown at 5×10^{-5} Torr, 650°C. The voids were formed by post-growth anneal in UHV at 750°C for the indicated times. Crystalline Si overgrowth was obtained for void areas exceeding 20×20 square nanometers.

ment in thermally grown ultrathin Si-oxide on Si (001)." According to this calculation, the kinetics are controlled by two separate surface reaction processes: Si monomer formation and SiO (gas) formation at the void perimeter. In contrast to previously published results, we found that these reaction steps have activation energies that are essentially indistinguishable as rate-limiting steps. For this reason, changing temperature is not expected to change the void formation kinetics.

C. Growth Techniques for Voided Ultrathin Oxides on Silicon (111) Developed

Void formation and growth experiments in ultrathin thermal oxides on the Si (111) surface exhibit similar behavior to that observed on Si (100). These results are summarized in Figure 5, where an increase in void density and size are also observed with anneal time. Interestingly, the formation of observable voids requires a longer time, suggesting that the void initiation on the (111) surface is more difficult than on the (100) surface. Like the (100) surface, the smallest oxide void areas found on the (111) surface (~29 nm^2) do not meet the specifications (3 to 12 nm^2) for oxide/silicon/oxide RTDs.

D. First Crystalline Silicon Overgrowth Demonstrated on Voided Oxides

Details of this demonstration are described in Appendix D. For the conditions indicated in Figure 4, with void areas of ~400 nm^2 (~23 nm diameter) and for a number density of ~2300/μm^2,

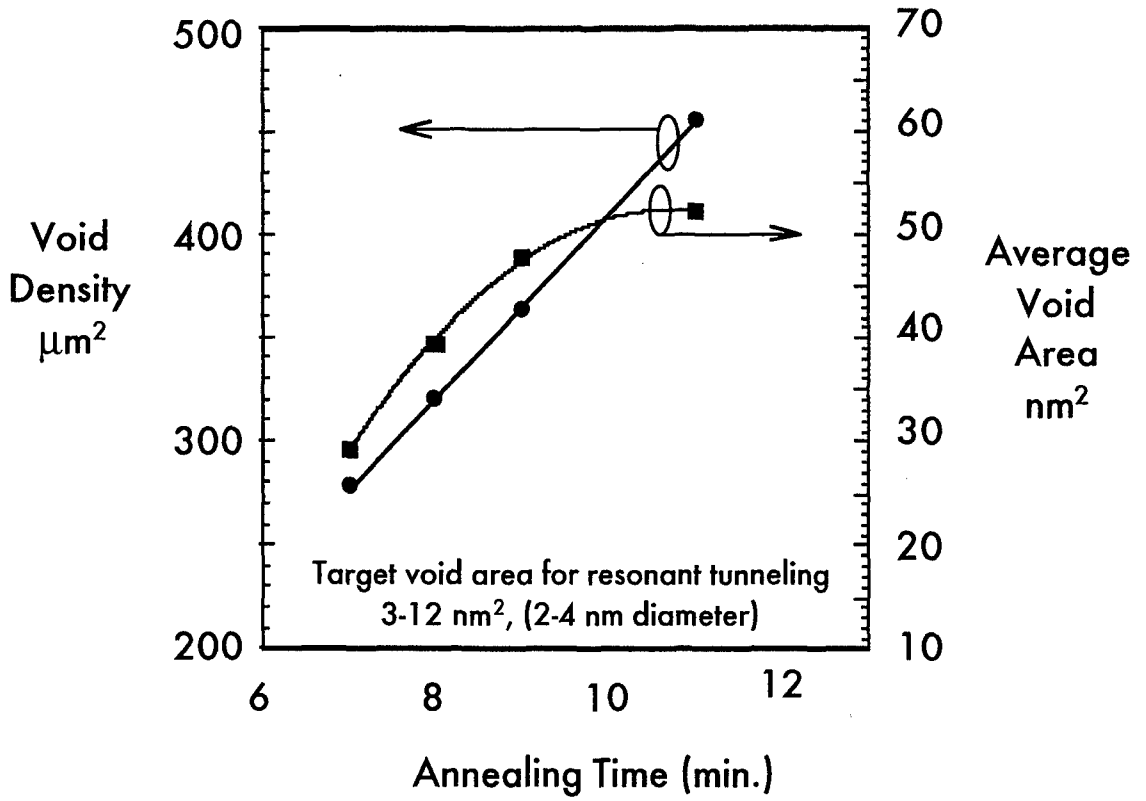

Figure 5. On the silicon (111) surface, dependence of the SiO_2 void density and size on the annealing duration: While smaller void areas can be obtained on the (111) surface compared to the (100) surface, void density is significantly smaller and not improved for forming SiO_2/Si/SiO_2 resonant tunneling structures.

overgrowth of single-crystal Si on voided oxide was achieved. As the void size decreases, the density of voids decreases, and we observe nanocrystalline silicon formation instead of single-crystal as indicated in Figure 4.

E. STM-Based Current-Voltage Measurements of Double-Barrier Structures

Current-voltage characteristics of crystalline and nanocrystalline quantum wells were measured using scanning tunneling microscope (STM) tips. Figure 6 shows a representative I-V measurement consisting of an averaged I-V response over the outlined areas. We found that localized I-V measurements of single- and double-barrier structures could exhibit negative differential resistance (NDR); however, when the I-V spectra were spatially averaged, no nonlocal tunneling resonances were observed. The observed NDR is not an unambiguous signature of resonant tunneling, as it could also result from tunneling into a surface state. Devices formed on these same materials also did not show clear evidence of resonant tunneling.

F. Ordered Silicon Nitride Growth Demonstrated on Si (111); Si Overgrowth Explored

Recently, the growth of an ordered silicon nitride film on Si (111) has been reported [2]; however, in the reported work, the feasibility of crystalline Si overgrowth on nitride was not ex-

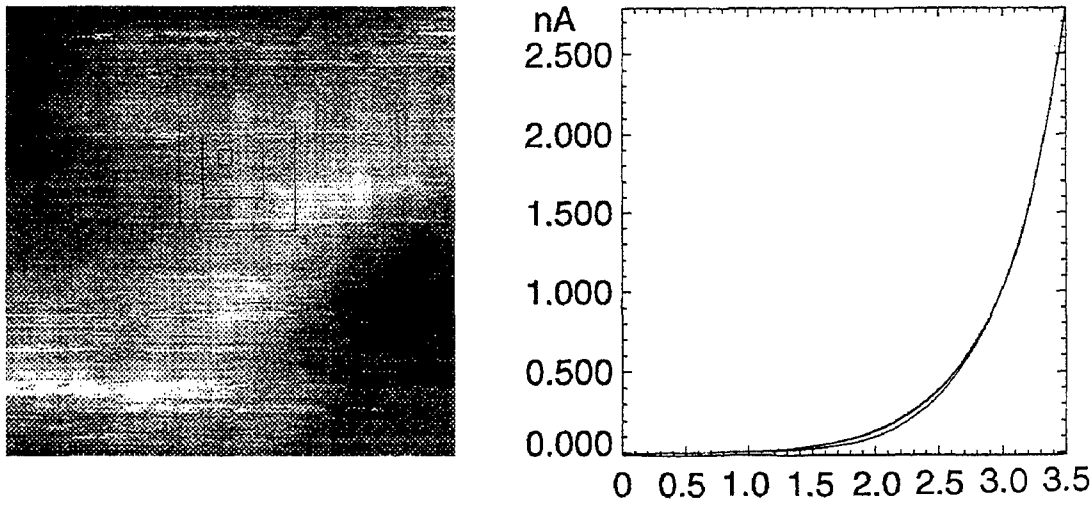

Figure 6. Oxide/silicon/oxide I-V silicon over voided oxide (*in situ* STM measurement).

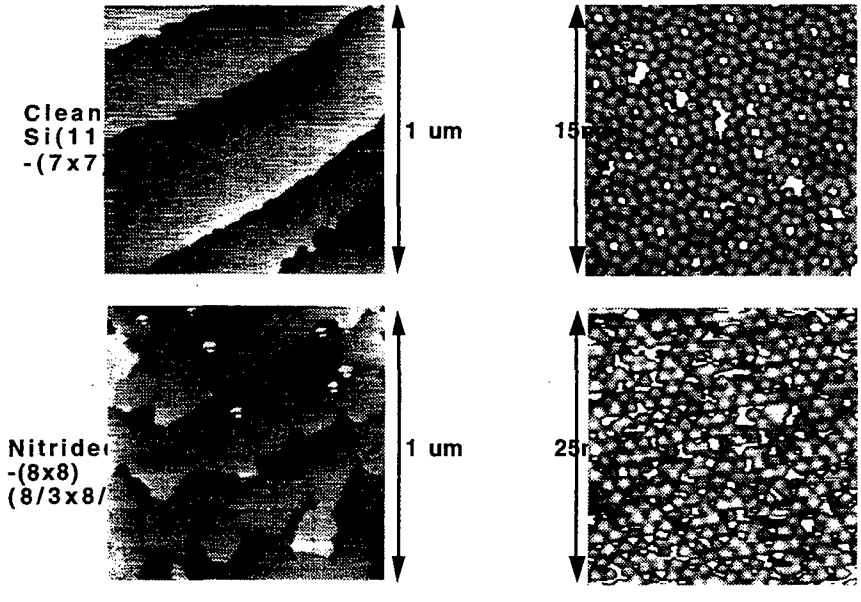

Figure 7. Void formation in ultrathin Si-oxide on Si (111). (Nitridation of Si (111) by NH_3 crystalline nitride layers; 6×10^{-7} Torr NH_3 at 950 °C for 2 minutes.

plored. Because of the potential for use of the ultrathin nitride as a tunnel barrier, we also experimented briefly with the nitride to see if we could reproduce the published result and overgrow crystalline Si. Our growth of the ordered silicon nitride is shown in Figure 7. On this nitride we surveyed the deposition of Si over a wide range of temperatures >600 °C but were unable to get Si to overgrow in crystalline form. Polysilicon growth could be the result of strain between the nitride and the Si over-layer. As single-crystal did not result, this approach was not pursued further.

G. Process and Mask Set Developed for Production of Oxide/Silicon/Oxide RTDs

A five-level mask set was designed to implement the process outlined in Figure 3; the process includes two electron beam lithography steps, to form the submicrometer oxide islands and

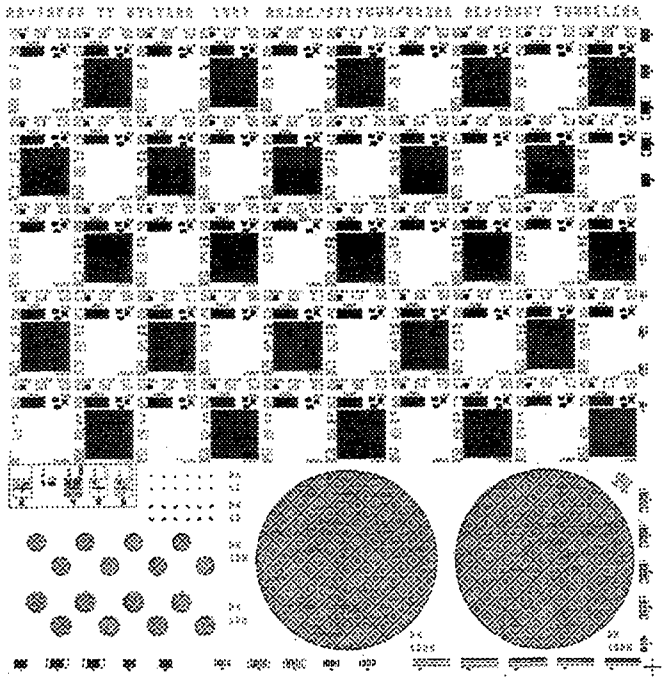

Figure 8. Oxide/silicon/oxide resonant tunneling diode mask layout. The actual size of the cell shown is 5.65 mm × 5.825 mm.

the emitters, and three projection optical lithography masks. The full mask is shown in Figure 8. Since the silicon overgrowth process is formed on micrometer- to submicrometer-scale oxide mesas and the RTD emitter contact areas are slightly below this, the current through a single RTD can easily become less than 10 fA (the approximate limit of our current measurement capability) if the oxide thicknesses become too large (~2 nm). For this reason, each cell of the mask contains arrays of the RTDs in addition to the single device: array sizes 10, 100, 1000, and 10,000 RTDs (labeled in Figure 8) allow parallel measurements of the average current through an RTD when the single device current is too low to be measured individually. Both square and circular RTD geometries are defined on the mask set with sizes and orientations as listed in Table 1.

Figure 9 shows an optical micrograph of four of the mask cells and an enlargement of the island array. This micrograph is from a process test run in which we used 50 nm thick silicon nitride islands. For these thick films, it is possible to see the island pattern optically. On the ultrathin oxides (1 to 5 nm), optical observance of the patterned film is not possible; the pattern is observable only in a scanning electron microscope (SEM) view.

Scanning electron micrographs of the overgrown oxide/silicon/oxide double barrier are shown in Figure 10. This image is taken after the emitters are deposited and before reactive ion etching to etch into the silicon and define the device areas; it is also taken in a region of the wafer from which the *in situ* aluminum deposition has been masked away. What can be seen in the lower right micrograph are 18 different RTD emitters, the first row with 0 degree orientation, the second row with a

15 degree orientation, and the third with a 30 degree rotation. About each emitter there is a dark ring that corresponds to the location of the first and underlying oxide island. The expanded region in the upper left was taken first and the charging of the second surface oxide is apparent in the second, lower right figure, where the charged surface has more emission than the previously uncharged surface. This is qualitative confirmation of the presence of the second oxide.

The measured room temperature current-voltage characteristics for a completed resonant tunneling oxide/silicon/oxide heterostructure are shown in Figure 11. The heterostructure consists of $SiO_2/Si/SiO_2/Al$ on n^+ Si with approximate dimensions of 2.5/3/1/20 nm. The n^+ Si side of the device is grounded and the top contact is voltage biased. For each measurement, the voltage starts at –1 V, ramps to +1 V, and then returns to –1 V. Some evidence of charging is observed for the 1 and 10 parallel RTD measurements for sweep rates corresponding to the medium integration rate of the HP4155 semiconductor parameter analyzer. Resonant tunneling is looked for in the forward (positive) bias polarity corresponding to tunneling in the direction of the Al metal contact. A factor of 10 increase is expected as the array size is increased; however, a large increase is observed between 10 RTDs and 100 RTDS. This is attributed to the e-beam proximity effect, which causes the areas of the RTDs fabricated in the arrays to develop out larger than the areas of the single and linear device strings. From Figure 11, we observe that the 100, 1000 and 10,000 device arrays have, as expected, approximately one order of magnitude differences in current, indicating that we have good uniformity of our array contact process.

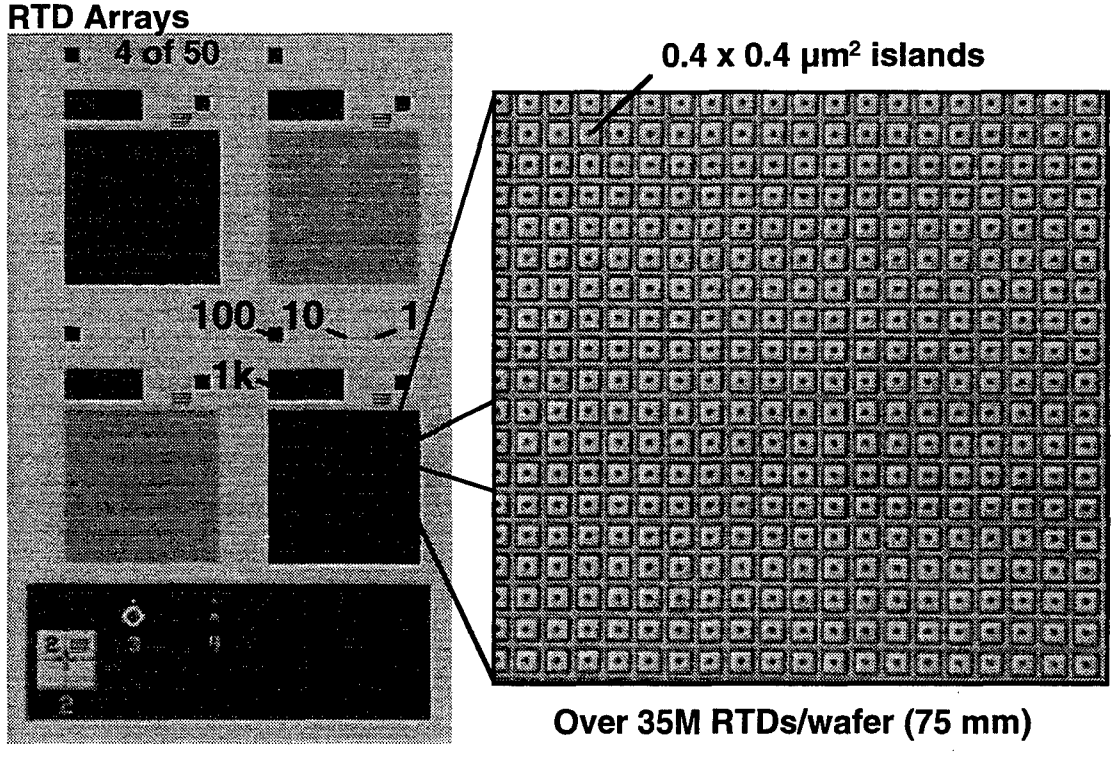

Figure 9. Optical micrograph of the resonant tunneling diode process shown after formation of submicrometer oxide islands.

Table 1. Key device parameters outlining the RTD device dimensions for the 50 different devices included on the mask set in Figure 8. The submicrometer oxide island is formed in two steps. First a pre-mesa pattern is formed to produce a large oxide mesa and clear the oxide from the greater surface of the wafer (75 mm). An e-beam step follows to form the submicrometer oxide island. The single-barrier device, SB10, characterizes the second oxide barrier only.

	Name	Mesa Width (μm)	Emitter-to-Mesa Separation	Emitter	Pre-Mesa
1	E01	0.3 × 0.3	0.1 × 0.1	0.1	2.2 × 2.2
2	E02	0.4 × 0.4	0.2 × 0.2	0.1	2.2 × 2.2
3	E03	0.5 × 0.5	0.3 × 0.3	0.1	2.2 × 2.2
4	E04	0.6 × 0.6	0.4 × 0.4	0.1	2.2 × 2.2
5	E05	0.7 × 0.7	0.5 × 0.5	0.1	2.2 × 2.2
6	E05A	0.8 × 0.8	0.5 × 0.5	0.15	2.2 × 2.2
7	E05B	0.9 × 0.9	0.5 × 0.5	0.2	2.2 × 2.2
8	E05C	1.0 × 1.0	0.5 × 0.5	0.25	2.2 × 2.2
9	E10	1.5 × 1.5	1.0 × 1.0	0.25	3.0 × 3.0
10	E10A	2.0 × 2.0	1.0 × 1.0	0.5	3.0 × 3.0
There are four of each of the above cells that correspond to rotation angles of 0, 15, 30, and 45, and one each of the circular emitter cells below, for a total of 49 RTDs.					
41	ED01	0.3	0.1	0.1	2.2 × 2.2
42	ED02	0.4	0.2	0.1	2.2 × 2.2
43	ED03	0.5	0.3	0.1	2.2 × 2.2
44	ED04	0.6	0.4	0.1	2.2 × 2.2
45	ED05	0.7	0.5	0.1	2.2 × 2.2
46	ED05A	0.8	0.5	0.15	2.2 × 2.2
47	ED05B	0.9	0.5	0.2	2.2 × 2.2
48	ED05C	1.0	0.5	0.25	2.2 × 2.2
49	ED10	1.5	1.0	0.25	2.2 × 2.2
50	SB10	None	1.0	No mesa	Single barrier

Note: Device-naming conventions: Ey means the emitter has an area of (0.y)2 square μm; EyRz means the emitter has an area (0.y)2, but the SiO2 island is rotated z degrees; EDy means the emitter diameter is 0.y μm; and SB stands for single barrier.

We can estimate the barrier thicknesses of the grown structure if we look more closely at the positive bias polarity and compare the current densities obtained in the double-barrier and single-barrier test structures with measurements we have obtained previously on single-barrier $n^+/SiO_2/Al$ heterostructures. Figure 12 shows a comparison of the current density measured through the 1 μm diameter and double-barrier devices. The single-barrier devices have the first oxide layer completely removed in the area in which they appear; these devices then consist of the growth of an undoped quantum well (4 nm) followed by ultraviolet ozone oxidation at room temperature. The

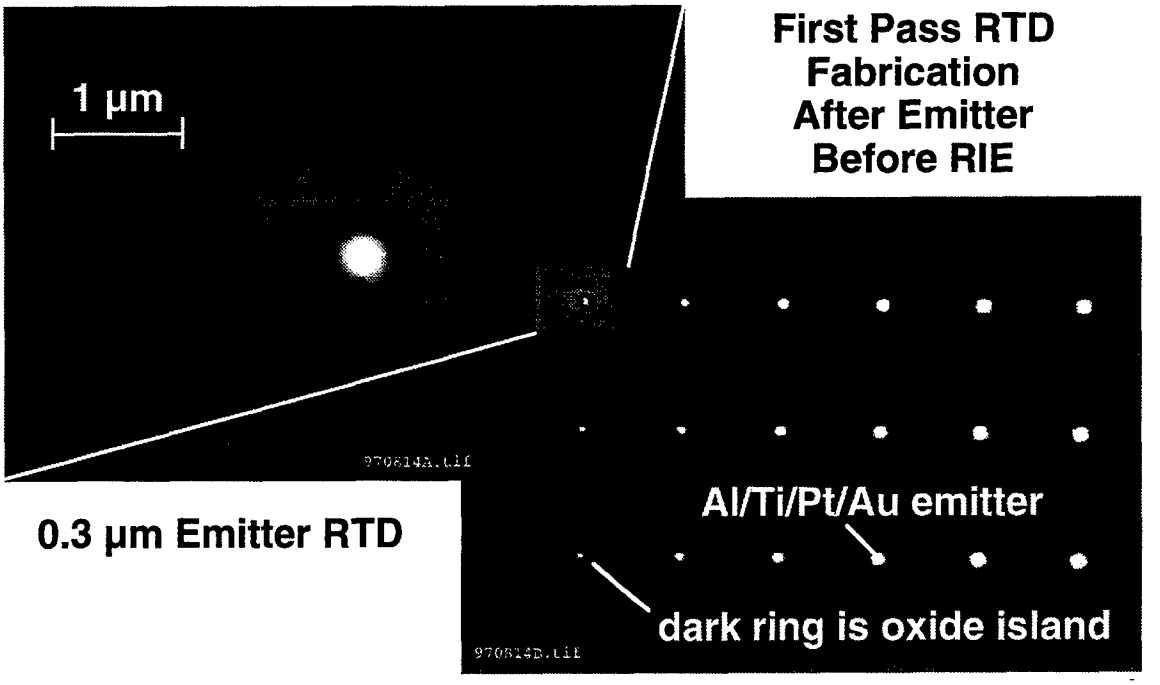

Figure 10. Scanning electron micrographs of the $SiO_2/Si/SiO_2$ resonant tunneling diode (wafer A4) taken after emitter formation over the double barrier. The first oxide islands are seen as dark regions about the submicrometer emitters.

UV-ozone oxide self-limits in thickness at about 1 nm. The oxide is then metallized with aluminum while still under vacuum and before removal from the growth/oxidation system.

The current density-voltage (J-V) characteristics for the single barrier can be seen in Figure 12 to correspond well with that of an oxide with thickness less than 1.6 nm, as expected. The J-V characteristic for the double barrier corresponds to an effective oxide thickness of about 2 nm, corresponding to a current density of about 10^{-2} A/cm^2. In simulation of tunneling in $Si0_2/Si/Si0_2$, we found that the resonant tunneling in these structures was not observable at room temperature until both barrier thicknesses were near 1 nm, corresponding to a current density exceeding 10^{-1} A/cm^2. Devices were being bonded for low-temperature measurements, but no resonance effects were observed, even at 4.2 K.

H. Demonstration of Interconnect Process for Low Current Density RTDs

The interconnect scheme was verified on a wafer of low current density, InP-based RTDs to demonstrate the process and to show that there are no measurement issues associated with characterization of large arrays of low current density devices. Figure 13 shows the I-V characteristics of the arrays with an order-of-magnitude increase in current for every 10× increase in array size. The RTDs are asymmetric, showing the low voltage resonance in only one bias polarity. An electron charge storage effect (Figure 13) was found in the low current density RTDs; this is intrinsic to the low current density III-V heterostructure.

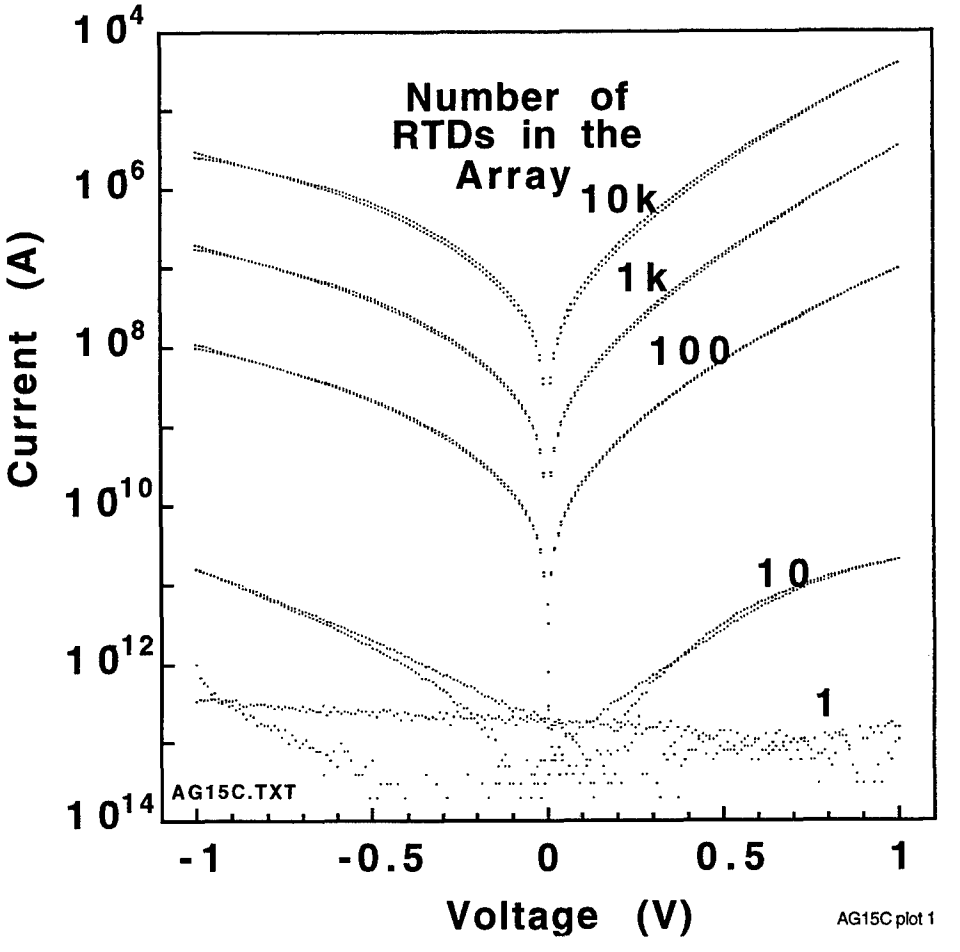

Figure 11. Measured current-voltage characteristics for an n^+ $Si/SiO_2/Si/SiO_2/Al$ resonant tunneling heterostructure with double-barrier dimensions of 2/3/1 nm at room temperature. The array numbers corresponding to the number of RTDs being tested in parallel (wafer A4, device ED05A, cell 4, 6; device diameters, 0.5 μm)

I. Conclusions

We explored two methods for forming $SiO_2/Si/SiO_2$ resonant tunneling diodes with crystalline silicon quantum wells. The first method, growth through voided oxide, was successful in demonstrating for the first time that crystalline Si can be grown through voids in the oxide. However conditions for forming the small void size needed to block electron transport, while allowing nucleation of silicon through the oxide, were not found. A systematic search of the growth temperature-pressure space showed that these conditions do not come naturally for the (100) and (111) surfaces. Off-orientation could be explored, but there is no theory to guide experiments and no good reason to believe the results will be significantly different. For this reason, we adopted a lateral-overgrowth approach in the final year to fabricate the RTD.

The $SiO_2/Si/SiO_2$ resonant tunneling diodes grown using the lateral silicon overgrowth process did not show the desired negative differential resistance characteristic, but tests on these diodes indicate that the desired heterostructure has not yet been achieved. Further optimization of the

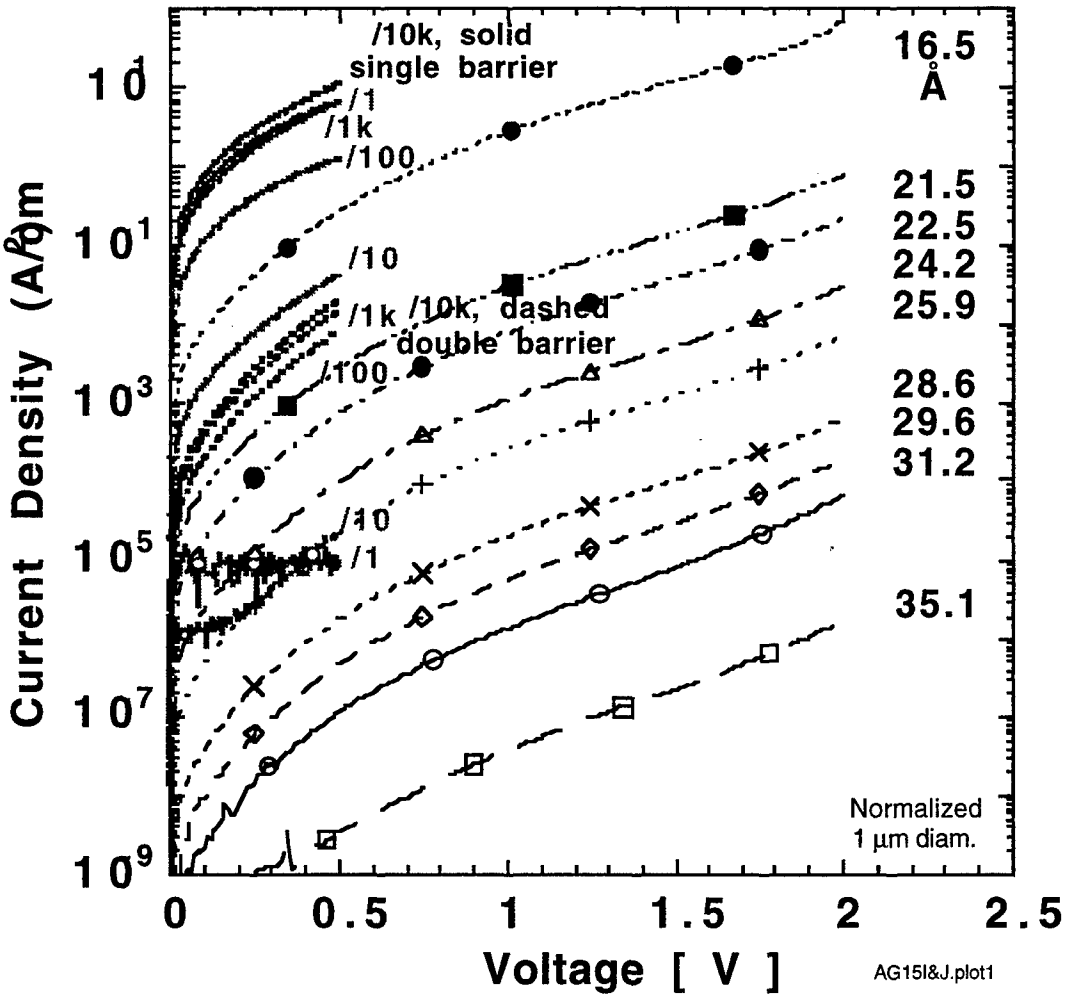

Figure 12. Comparison of the measured single- and double-barrier diodes against the measured characteristics of single-barrier Si/SiO_2/Al tunnel diodes from reference [3]. The curves from reference [2] are shown in the range 0 to 2 V; the new measured data (for various array sizes) were taken from 0 to 0.5 V (wafer A4; device diameter, 1 μm).

overgrowth process is needed to demonstrate the RTD. This process has now been transferred to DARPA's Si-Based Quantum MOS Technology Development program (Contract No. F49620-96-C-0006), where it will be used for lateral overgrowth of RTD heterostructures.

Appendix F, "Beyond-the-roadmap technology: Silicon heterojunctions, optoelectronics, and quantum devices," addresses future prospects for silicon heterojunctions and their potential for use in device scaling and in silicon substrate, quantum well, and optical device applications.

IV. PERSONNEL SUPPORTED

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Raytheon Systems Company

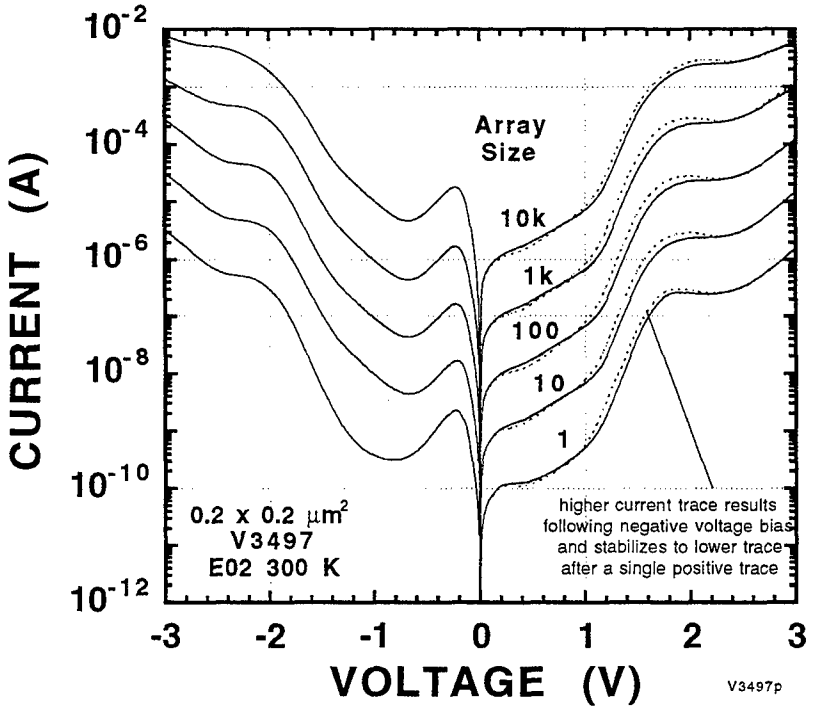

Figure 13. Demonstration of RTD array contact process on III-V resonant tunneling diodes.

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V. PUBLICATIONS

Robert M. Wallace and Shaoping Tang, "Designing materials by first-principles computational methods," *Texas Instruments Technical Journal* 12 (1995), p. 66.

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Glen D. Wilk, Yi Wei, Hal Edwards, and Robert M. Wallace, "*In situ* flux cleaning technique for producing atomically flat Si (100) surface at low temperatures," *Applied Physics Letters* 70 (1997) p. 2288.

Shaoping Tang, Yi Wei, and Robert M. Wallace, "Energetics of void enlargement in thermally grown ultrathin Si-oxide on Si (001)," accepted for publication in *Surface Science Letters* (1997).

Shaoping Tang, Robert M. Wallace, Alan Seabaugh, and Dominic King-Smith, "Band offset of ultrathin SiO_2.Si (001) interface: a first-principles study," to be submitted to *Applied Surface Science* (1997).

VI. INTERACTIONS/TRANSITIONS

Presentations at Conferences (for the period 1 September 1994 – 31 August 1997)

Presented at the American Physical Society March Meeting, St. Louis, MO:

"Evolution of Si (100) Surface Morphology During Thermal Annealing and Post-Oxidation Annealing," Yi Wei, Robert M. Wallace, and Alan Seabaugh

"Electronic Structure of the Ultrathin SiO_2/Si(100) Interface: A First Principles Study," Shaoping Tang, Robert M. Wallace, Dominic King-Smith, and Alan Seabaugh.

Presented at the Si-Nanoelectronics Workshop in Honolulu, HI, June 1996:

"Controlled Growth of Si-Oxide Barriers for Si-Based Resonant Tunneling Devices," Yi Wei,

Shaoping Tang, Robert M. Wallace, and Alan Seabaugh

Presented at the Gordon Conference on Chemical Reactions at Surfaces, Ventura, CA, March 1997:

"Energetics of Void Formation in SiO_2 on Si (100)," Robert M. Wallace, Shaoping Tang, and Yi Wei

Presented at the Materials Research Society, Boston, MA, December 1997:

"Beyond-the-Roadmap Technology: Silicon Heterojunctions, Optoelectronics, and Quantum Devices" (Invited)

VII. NEW DISCOVERIES, INVENTIONS, OR PATENT DISCLOSURES

Filed with USPTO 18 March 1996: "Method to produce ultrathin porous silicon-oxide layer," TI-22384.

Filed with USPTO 18 March 1996: "Method to produce ultrathin porous silicon-oxide layer employing island nucleation," TI-22978.

Filed with USPTO 14 August 1996: "Method to produce pin-hole-free, high-quality Si (100) surfaces using Si-flux cleaning," TI-22960.

Disclosure date 23 May 1997: "Method to grow crystalline silicon overlayers on thin amorphous silicon dioxide layers at low temperature for the purpose of resonant tunneling diodes," TI-26176.

VIII. HONORS/AWARDS

None.

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Appendix A

Band offset of ultrathin SiO_2.Si (001) interface: a first principles study. To be submitted to *Applied Surface Science* (1997).

Band offset of ultrathin SiO_2/Si(100) interface: a first-principles study

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Abstract

Using a first-principles pseudopotential approach, we have studied SiO_2/Si(100) superlattice structure constructed between β-cristobalite SiO_2 and Si(001). Three superlattices containing 2, 4 and 8 layers of SiO_2 are considered. The results showed that once the Si dangling bond is properly saturated, no electronic states are present within the fundamental gap. The calculated conduction band offset between Si and SiO_2 is found to increase with oxide thickness and reach a saturation value beyond the 4 layers of SiO_2.

Introduction

The critical role of silicon dioxide and its interface with silicon for metal-oxide-semiconductor (MOS) technology can never be overemphasized. The physical and electronic properties associated with the SiO_2/Si interface determines the fundamental device operational parameters. As MOS critical dimensions continue to scale down, there is an increasing need to fully understand the physical and electronic structures of the SiO_2/Si interface.

Unfortunately, much remains to be understood about the detailed interface atomic and electronic structure, despite a great deal of efforts to grow thin-oxide layers on Si surface in the last three decades. Previous studies generally supported an interface model with a non-stoichiometric transition region separating crystalline Si and amorphous SiO_2. However, a flurry of recent experiments showed evidence that an abrupt and ordered interface structure between Si and SiO_2 is formed. Theoretical simulations of such interface had been hampered partly by the uncertainty and complexity of the interface structure.

The core-level spectroscopy measurement on SiO_2/Si interface showed that there are suboxide species at the interface[1]. TEM and X-ray reflectivity studies showed the evidence of ordered structure in the Si/SiO_2 interface[2,3]. A recent theoretical calculation by Pasquarello, Hybertson and Car [4] on a model SiO_2/Si interface derived from tridymite SiO_2 grown on Si(100) provides a detailed analysis of bond length and bond angle distributions at the interface. Their results also suggested that a transition region which is similar to amorphous bulk SiO_2 exists at the SiO_2/Si interface. These studies contribute substantially to the understanding of the atomic and electronic structure of SiO_2/Si, although none of the proposed structures has been unambiguously accepted.

In this work, we aim at gaining a basic understanding of the electronic properties of SiO_2/Si interface using a structural model proposed by Herman, Batra and Kasowski[5] (thereafter referred as HBK model). We studied three superlattice structures containing alternate Si and SiO_2 layers as a function of varying the thickness of the included SiO_2 layers. Because of the way the model is constructed, a Si dangling bond exists at the interface within a unit cell. Himpsel et al. [1] suggested using H, O or OH to saturate the Si dangling bond. Our study showed that a single hydrogen atom is unable to perform the complete saturation of a dangling bond in the HBK model. On the other hand, a single oxygen can form a double bond with a Si and completely saturates the Si dangling bond. This O saturation leaves no interface states in the fundamental gap of the superlattice.

Methodology and models

We used a first-principles plane wave pseudopotential method[6] based on the local density approximation (LDA) to density functional theory. The exchange-correlation energy is calculated using a parameterized form of the exchange-correlation energy[7] of the homogeneous electron gas obtained using quantum Monte Carlo techniques[8]. Norm-conserving pseudopotentials constructed within the scheme developed by Troullier and Martin[9] are used. The wave functions are expanded in a plane-wave basis set with an energy cutoff of up to 30 hartrees. One special k point is used for sampling k space[10].

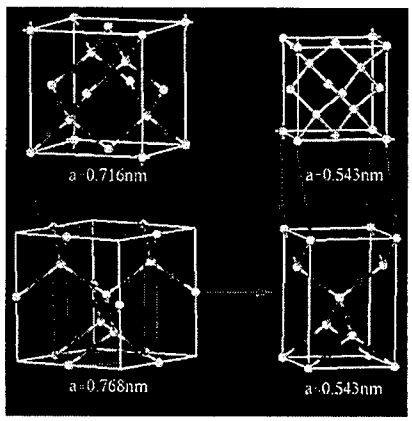


Figure 1: The construction of HKB SiO_2/Si interface model.

The Si/SiO_2 interface is constructed according to the HKB model[5] assuming that a β-cristobalite SiO_2 is epitaxially grown on Si(001) surface, shown in Figure 1. By rotating the unit cell of β-cristobalite by 45°, one can get a smaller tetragonal unit cell which can align with Si(001) substrate provided that the lattice constants of this tetragonal cell is the same with Si. In practice, we expand the SiO_2 lattice constant by 6.8% to allow an epitaxial growth of SiO_2 on Si(001). The virtue of this model is its relative simplicity and the ease of incorporating various chemical imperfections at or near the interface. Additionally, the strain imposed on the SiO_2 structure, relative to the Si lattice (6.8% lattice mismatch), is smaller than other known phases of SiO_2. Previous experimental studies also suggest that this structure may be close to the real interface structure. Figure 2 shows the three structural models we used in the calculation. Each model has four Si layer sandwiched between SiO_2. The smallest structure is $(Si)_4(SiO_2)_2$ which contains 2 SiO_2 layers of thickness of 3.8Å and the largest structure is $(Si)_4(SiO_2)_8$ that contains eight layers of SiO_2 with a thickness of 15.4Å. An alternative interface model based on the

tridymite SiO_2-Si interface has been studied theoretically by Pasquarello, Hybertsen and Car[4]. However, the mismatch between tridymite SiO_2 and Si is much larger than that from cristobalite (~12%).

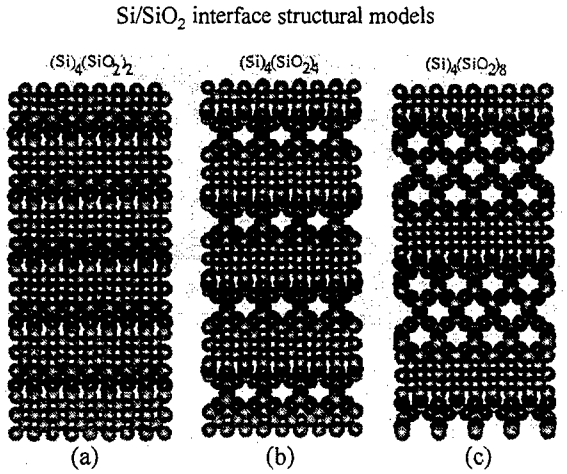


Figure 2: Three SiO_2/Si interface models used in the calculation.

Results and discussion

Band structures

We start with a $(Si)_4(SiO_2)_2$ superlattice structure shown in Figure 2(a). At the Si-SiO_2 interface, there are two Si dangling bonds pointing to the oxide. Initially, these dangling bonds were saturated by oxygen. Without considering the lattice relaxation, the calculation showed that there is an indirect fundamental gap of 0.56eV. The actual bandgap, of course, should be larger than 0.56eV as it is well known that LDA theory always underestimates excited state properties such as the band gap. If the atomic positions are fully relaxed, the bandgap is still indirect, but the calculated gap size is increased to 0.7eV. This result shows that an unrelaxed (i.e. strained) interface structure has smaller bandgap than the relaxed structure.

We also performed the calculation on $(Si)_4(SiO_2)_2$ structure by using H to saturate the Si dangling bonds at the interface. The purpose of such study is to simulate the effect of a H impurity on the electronic band structure, since hydrogen incorporation is unavoidable in the materials processing. We find that H does affect the band structure by introducing two interface states within the forbidden band. These states fill the bandgap and make this Si-SiO_2 superlattice model exhibit metallic electronic behavior.

In another attempt to simulate the various interface conditions, we studied the structure $(Si)_4(SiO_2)_2$ assuming that Si dangling bonds are not saturated at the interface. The results show that two unoccupied surface states appear in the forbidden band. These surface states can readily interact with any impurities at the interface and introduce unwanted electronic states.

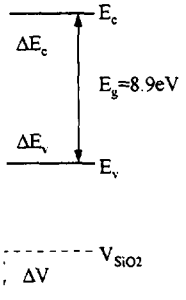
In order to evaluate the effects of thickness variation of the SiO_2 layer on the overall band structure, we studied a four layer SiO_2 superlattice structure (ie. $(Si)_4(SiO_2)_4$) shown in Figure 2(b)) while the Si layer is kept the same as the previous two layer SiO_2 HKB structure. The calculation is done without considering the lattice relaxation. The results show that this four

tructure has an indirect bandgap of 0.91eV which is 0.35eV larger than that of O_2 HKB structure. This result, coupled with the fact that bulk SiO_2 has a , suggests that the bandgap of SiO_2-Si superlattice increases with the thickness

ılation

ɜ most important parameters characterizing heterojunctions are the valence and discontinuities (or band offset). The knowledge of these quantities is essential ıe transport properties of the interface, or the electrostatic potential in a vice. A main problem in calculating the band discontinuity is to correctly line ıe two materials at the interface. This information can not be obtained from the alone because no absolute energy reference is defined in a infinite solid

come the band line up problem was developed by Van de Walle and Martin to calculate the average potential for each bulk material and then calculate the om one material to another at the interface from a combined heterojunction a superlattice structure. The potential shift between the two materials is used to ɔetween the average potential of each bulk material. Figure 3 illustrates this idea terface as an example. The average potential of each bulk material (i.e. Si and ɜd by a potential ΔV which is calculated from the Si/SiO_2 superlattice. The ıduction band offset can then be obtained based on the band gap value and the ;ition (E_V) relative to the average potential for each material.



natic representation of band lineups. The calculated potential shift (ΔV) across termines the lineup of average potential in the bulk.

potential shift and the corresponding valence (ΔE_V) and conduction (ΔE_C) band interface models are listed in Table 1. It can be seen that the conduction band along with the increase of the oxide thickness. It has to be emphasized that these for determining trends and not for quantitative description (values) of the band for the $(Si)_4(SiO_2)_2$ model where only two layers of SiO_2 is included, the l offsets have potentially large error because the band gap of this thin SiO_2 layer is reasonable to assume that the bandgap of this thin oxide region is smaller than d gap (8.9eV). Thus, the conduction band offset result for this model (1.71eV) is actual value. Another error in such calculations comes form the models assumed

because these were constructed using a expanded SiO_2 lattice (with 6.8% expansion) stacked on Si(001) (Figure 1). The uncertainty of the band gap of the expanded SiO_2 will also introduce some error in the calculation. Our calculations showed that the expanded SiO_2 lattice will have smaller band gap than the regular SiO_2 lattice. As a result, the band offset result in Table 1 will becomes smaller.

Table 1: The potential shift (ΔV) across the Si/SiO_2 interface and the valence and conduction band offset for three different structural models.

interface	$(Si)_4(SiO_2)_2$	$(Si)_4(SiO_2)_4$	$(Si)_4(SiO_2)_8$
ΔV (eV)	0.65	5.85	5.85
ΔE_V (eV)	6.02	0.82	0.82
ΔE_C (eV)	1.71	6.91	6.91

To estimate the effect of an expanded SiO_2 lattice on the band offset calculation, we studied the bandgap of a regular SiO_2 bulk and an expanded SiO_2 bulk with a 6.8% expansion of regular lattice constant of a SiO_2. The calculated band gaps are 5.46eV and 4.70eV respectively. Thus, it is not surprising to see that the calculated band gap (5.46eV) of SiO_2 is smaller than the experimental result (8.9eV), because of the well known underestimation of band gap by LDA method. To adjust the calculated band gap to experimental result, a factor of 1.63 is used to bring the theoretical band gap result in line with the experimental result. Using the same factor, we can obtain the estimated band gap of the 6.8% expanded SiO_2 lattice to be 7.66eV. If this band gap result is used, the conduction band offsets are shown in Table 2. Compared to Table 1, it can be seen that all conduction band offsets are shifted down.

Table 2: Revised valence and conduction band offset for three different structural models at Si/SiO_2 interface.

interface	$(Si)_4(SiO_2)_2$	$(Si)_4(SiO_2)_4$	$(Si)_4(SiO_2)_8$
ΔE_V (eV)	6.02	0.82	0.82
ΔE_C (eV)	0.47	5.26	5.26

An important result from the present study is that the band offset reaches a saturation value after four layers of Si-oxide which is about 7.5Å. This shows that the thin Si-oxide film will therefore have bulk-like electronic properties after this thickness. Atomic relaxation studies on $(Si)_4(SiO_2)_2$ and $(Si)_4(SiO_2)_4$ models showed a large atomic relaxation within the 7.5Å region.

In summary, we have studied the electronic structure of $Si\text{-}SiO_2$ interface using a first-principle pseudopotential method. The results showed that no electronic states are present within the fundamental gap. An important conclusion is that the conduction band offset increases with the thickness of the oxide and reaches a constant value beyond 7Å oxide thickness. Our study also shown that a relaxed superlattice structure yield larger bandgap than a strained superlattice.

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Appendix B

***In situ* flux cleaning technique for producing atomically flat Si (100) surface at low temperatures, *Applied Physics Letters* 70 (1997) 2288.**

In situ Si flux cleaning technique for producing atomically flat Si(100) surfaces at low temperature

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(Received 4 November 1996; accepted for publication 28 February 1997)

We have developed a method for removing oxides and producing atomically flat Si(100) surfaces with single atomic height steps using a Si flux cleaning technique. By introducing a Si flux in the range 1.0–1.5 Å/s at the onset of an SiO_2 thermal desorption step as low as 780 °C, scanning tunneling microscopy (STM) and atomic force microscopy images reveal smooth surfaces with atomically flat terraces with an rms roughness of 0.5 Å and single-step heights of 1.4 Å. STM reveals that A- and B-type steps are present across the entire area of the scanned surface. Desorption of the surface oxide layer with Si fluxes below this range results in rougher surfaces with pits ~50 Å deep and 1000 Å across. For Si fluxes above this range, no pits are seen but atomic steps are not visible on the surface. © *1997 American Institute of Physics.* [S0003-6951(97)04017-5]

Device scaling in CMOS is requiring ever thinner gate oxides while still demanding high reliability of these oxides. The gate oxide thinning trend is now placing more focus on the interface between the SiO_2 layer and the Si substrate as a means of identifying the sources of premature breakdown and perhaps improving reliability.[1–3] The interface roughness depends strongly on the cleaning procedure used in preparing the Si surfaces, and standard techniques[4,5] of producing a surface oxide cap followed by an *in situ* anneal step at 800–900 °C can actually produce pits on the surface which are 50 Å deep and up to 1000 Å across. For thin-film growth, this large roughness can significantly affect the properties of the film.

It has been suggested for thick oxides[6–8] (~200 Å) and for thin oxides[9–12] (≤30 Å) that the pits form by SiO etching of the substrate, where suboxides (SiO_x, $0<x<2$) near the interface desorb as volatile SiO molecules, followed by reduction of the oxide layer in the reaction $SiO_2+Si \rightarrow 2SiO$ (g). Mobile Si monomers are suggested[10] to form in the substrate voids left by the suboxides near the interface which then reduce SiO_2 molecules to the volatile SiO form, which desorbs from the substrate. Engel *et al.*[9] has also argued through energetics considerations that the formation of mobile monomers is the rate-limiting step in the reaction. Recent investigations on the void growth process, however, suggest that mobile Si monomer formation and SiO formation are kinetically competing processes on the Si surface.[13] While this method removes the oxide, it does so at the expense of forming pits in the Si substrate. It is very desirable, however, to remove the oxide without forming pits in the substrate and also without using chemical etching. Removing the chemical etching steps could reduce and simplify the number of surface preparation steps used in standard processing procedures. Further, while HF etching removes the oxides and yields a smooth, H-terminated surface (rms roughness ~1 Å), there is no well-ordered structure to the surface. An atomically flat Si surface with well-ordered steps can be obtained by flashing the sample at 1200 °C but this process is not practical for large wafers and thermal budget concerns.

A typical surface preparation method starts with the formation of a chemical oxide as a protective cap on the Si surface. Once the sample is placed in vacuum, resistive or radiative heating is used to anneal the sample at 800–900 °C for several minutes to desorb the oxide. Various low Si deposition rates (~0.1–0.6 Å/s) have also been used[14–16] for several minutes in an attempt to improve the surface quality for subsequent thin-film growth. While the emergence of reflection high-energy electron diffraction (RHEED) streaks and spot patterns was used as an indication of oxide removal in some of these studies, it was assumed that these processes yield a flat, uniform surface. Under many oxide desorption conditions, however, a rough surface can result which may have a significantly detrimental effect on ultrathin film properties, particularly where a uniform interface is required. To our knowledge no one has investigated the Si surfaces with atomic resolution probes following these treatments. An *in situ* Si surface cleaning technique which uses relatively low temperatures and yields an atomically flat, stepped surface is very desirable. In this letter, we describe a Si flux cleaning technique which can be used to obtain atomically flat, single-height steps on Si(100) at temperatures between 700 and 800 °C. The surface cleaning conditions have been varied as a function of Si deposition rate and substrate temperature.

The substrates were nominally flat 4-in Si(100), *n*-type wafers with $\rho=0.01–0.02\ \Omega$ cm. Some of the as-received wafers were placed directly into a molecular beam epitaxy (MBE) chamber without any *ex situ* chemical cleaning, while others received an initial degreasing with acetone and methanol. The substrates where heated radiatively by a strip heater near the backside of the wafer. A thermocouple placed near the substrate was used for temperature measurements. Since the substrate holder rotates during the surface preparation procedure, direct contact between the thermocouple and substrate was not possible. The thermocouple was calibrated to an optical pyrometer over the temperature range used in this experiment. While the temperature reproducibility was ±5 °C, the absolute temperature is accurate to ±25 °C. After a long degas at 400 °C, the wafers were heated up to 650 °C, at which point the wafer surface was exposed to the Si flux. The anneals were then done at various temperatures and times while the Si flux impinged on the substrate. The base pressure in the MBE chamber was 5×10^{-11} Torr, and was $\sim8\times10^{-10}$ Torr during Si deposition. Following the Si flux

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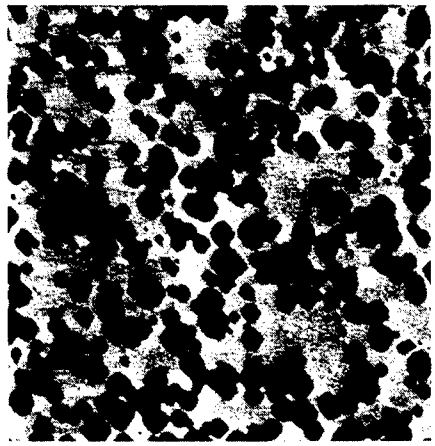

FIG. 1. 10×10 μm^2 AFM image of Si(100) with a native oxide which has been partially desorbed by annealing at 780 °C for 30 min. A high density of voids (1000–5000 Å wide, 40 Å deep) is seen on the surface.

cleaning step, the wafers were removed from vacuum, cleaved and transferred in air as rapidly as possible (no longer than 30 min) for STM (in UHV after transfer) and atomic force microscopy (AFM) (in ambient, performed in "tapping" mode) analyses.

Figure 1 shows a 10×10 μm^2 ambient AFM image of a Si(100) surface which has undergone a partial thermal desorption of the native oxide. The sample was heated at 780 °C for 30 min under UHV conditions. A very high density of holes is clearly seen across the surface. The holes range from ~500 to 5000 Å wide and are ~40 Å deep. The initial native oxide is still present in the regions between the holes. With no Si flux provided during the anneal step, it is seen that a rough, nonuniform surface results.

Figure 2(a) shows a 10×10 μm^2 AFM image of a Si(100) surface (initially containing a native oxide) which has been annealed at 780 °C for 30 min, with a Si flux (~0.3 Å/s of Si) being introduced for the *final* 10 min of the anneal only. While etching of the substrate still occurs, the void density and size have been reduced by the addition of a Si flux during the anneal. Figure 2(b) shows a 5000×5000 $Å^2$ UHV STM image of the sample in Fig. 2(a). Compared to the surface in Fig. 1, the surface is much smoother between the voids, and the voids themselves are much better defined: there is clearly a four-fold symmetry to the voids, reflecting the symmetry of the Si(100) substrate. The addition of a Si flux has resulted in a clean surface and the formation of a well-defined step structure corresponding to the original miscut angle of the surface. This indicates that although the addition of a Si flux for the final 10 min helps to reduce the void size and density, it does *not* prevent void formation. The holes also appear to act as step pinning centers, as the image shows several steps with very small terrace widths near the hole edge. This behavior may contribute to the depth of the holes in addition to substrate etching by SiO formation.

Figure 3 shows a 1×1 μm^2 STM image of a Si(100) surface (initially containing a native oxide) which has been annealed at 780 °C for 10 min, with the Si flux (~1 Å/s) being introduced at the *onset* of the thermal anneal (at 650 °C, followed by a temperature ramp up to 780 °C). No holes are visible (larger-area scans show no holes across 100

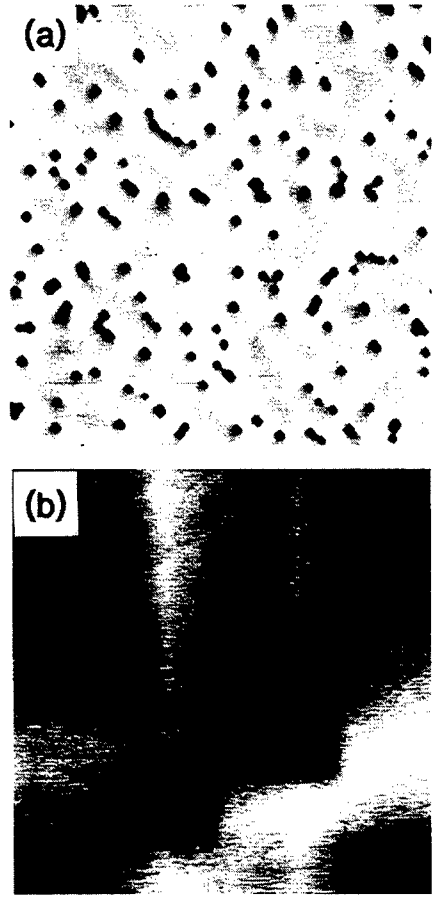

FIG. 2. (a) 10×10 μm^2 AFM image of Si(100) after complete desorption of the native oxide. The sample was annealed at 780 °C for 30 min with a Si deposition rate=0.3 Å/s being introduced for the *final* 10 min of the anneal. (b) 0.5×0.5 μm^2 STM image of the sample in Fig. 2(a). The holes reflect the four-fold symmetry of the substrate and act as step pinning centers.

μm^2 in AFM). The measured rms roughness is 0.5 Å for this image. Alternating A-type (smooth) and B-type (rough) steps can be seen in the image which indicates a smooth, high quality surface with 1.4 Å single atomic height steps. This image reveals an extremely well-defined step structure on the surface. Atomically flat surfaces such as this one were observed for all samples which were Si flux-cleaned with the Si deposition rate between 1.0 and 1.5 Å/s.

Most Si cleaning methods which use Si deposition to improve the surface quality introduce a Si flux at some point after the heating has been initiated, and often it is done after the anneal step has been completed. This work demonstrates, however, that it is critical that the Si flux be started at the *onset* of the heating step, in our case 650 °C, so that reduction of the oxide at the top surface prevents oxide reduction at the interface. It is also essential that Si is deposited at an appropriate rate to compete with the interfacial reduction reaction. For Si deposition conditions outside of the range of 0.2–2 Å/s, the surface becomes significantly rougher. For Si deposition rates below ~0.2 Å/s, Si is not supplied quickly enough to reduce SiO_2 from the top surface, and voids form from reaction at the bottom SiO_2 interface. For deposition rates higher than ~2 Å/s, Si deposits too quickly for the decomposition to occur, thus excess Si blankets the surface and creates less well-defined steps. It is also possible that not all of the SiO_2 is desorbed in this case, which would account

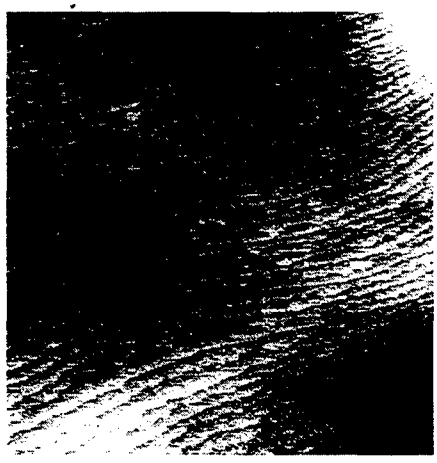

FIG. 3. 1×1 μm^2 STM image of Si(100) after desorption of the native oxide at 780 °C for 10 min with a Si flux of ~1 Å/s, introduced at the *onset* of the thermal desorption step. The measured rms roughness is 0.5 Å and both A-type and B-type single atomic height steps can be seen.

FIG. 4. 1×1 μm^2 STM image of a Si sample initially containing a native oxide after an anneal at 800 °C for 10 min with a Si flux of 6 Å/min. A highly nonuniform surface results with a high density of large holes. The inset shows the corresponding RHEED pattern taken from this surface.

for the less well-defined surface structure. The optimum Si deposition rates were found to be 1.0–1.5 Å/s, where STM and AFM both observed atomically flat terraces and single-height A- and B-type steps (as seen in Fig. 3). Within this range, it appears that the Si monomer arrival rate is balanced with the SiO_2 reduction rate and a high-quality surface can be obtained.

These results indicate that at low deposition rates a rough, very nonuniform surface results. We reproduced previously reported cleaning conditions by preparing a sample with an anneal step at 800 °C for 10 min and a Si flux of ~6 Å/min, which closely approximates the rate of ~8 Å/min at 800 °C as suggested by others.[15] Figure 4 shows a 1×1 μm^2 STM image of the surface under these conditions. It can be seen that the surface is marked by a very high density of pits which are ~50 Å deep. The inset of Fig. 4 shows the corresponding RHEED pattern from this surface, which contains streaks normally associated with a smooth, reconstructed crystalline surface. Although RHEED is often used as an indicator for smooth, uniform and crystalline surfaces, defects of this type will yield a deceptive RHEED pattern which may be mistaken for a high-quality surface. The presence of pits is expected only to decrease the intensity of and slightly broaden the RHEED spots.[17] It is clear that this type of RHEED pattern may be incorrectly interpreted without STM examination of the surface. These surface nonuniformities can have a profound effect on any subsequent film growth.

At substrate temperatures up to 900 °C, the surface maintains sharp single-height steps and atomically flat terraces. This behavior is not surprising, as an increased Si adatom diffusion length maintains high surface quality. At much higher temperatures, however, it is expected that surface roughening will occur during deposition. High-quality surfaces have also been observed down to temperatures of 700 °C, although the step edges are not as well defined and the terraces show more roughness. Within large windows of deposition rate and substrate temperature, very high-quality Si surfaces can be obtained using this technique.

This method appears to work well because the oxide reduction reaction at the surface has one less reaction step than that at the interface. Since the Si atoms arrive uniformly as monomers in the flux, the activation barrier for Si monomer formation is removed. Recent calculations suggest[18] that the activation energy for Si monomer formation from the 2×1 reconstructed surface is comparable to that for reduction of SiO_2 to SiO. If this is the case, the reaction at the oxide surface may occur more rapidly than the interface reaction. For very thin oxides ($\leq$30 Å), the SiO_2 layer can be completely removed before voids of significant size form at the interface. For thicker oxides (>30 Å), significant reduction of the oxide may be unavoidable by this technique, but the Si flux cleaning method should work well for oxides formed in air and by standard chemical cleaning procedures.

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Appendix C

Void formation on ultrathin thermal silicon oxide films on the Si (100) surface, *Applied Physics Letters* 69 (1996) 1270.

Void formation on ultrathin thermal silicon oxide films on the Si(100) surface

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The formation of voids on the thermally grown (650 °C) ultrathin (~1 nm) silicon oxide films on the Si(100) surface was investigated by using ultrahigh vacuum scanning tunneling microscopy. Voids form randomly on the ultrathin oxide film upon thermal annealing at 750 °C. In contrast to void formation observed on thicker (>5 nm) thermal silicon oxide films and that observed on ultrathin (~1 nm) oxide films formed by room temperature O_2 adsorption, the number of voids increases during annealing. We find that Si monomer creation *and* SiO production compete kinetically in the void formation process. © *1996 American Institute of Physics.* [S0003-6951(96)02735-0]

The ultrathin silicon oxide film and its interface with silicon have drawn increased attention in recent years due to the continued scaling of metal–oxide–semiconductor (MOS) device technology. Transistors with ultrathin gate oxides well within the direct tunneling regime (≤3 nm) have been recently demonstrated.[1] Moreover, prospects for Si-based nanoelectronic devices, such as resonant tunneling diodes, depend critically on the control of ultrathin, Si-compatible tunnel barrier materials.[2] The thermal stability of ultrathin oxide films is a prerequisite to the production of either of these devices.

Void formation on thermally grown oxide films,[3–5] ultrathin oxide films formed by room temperature O_2 adsorption,[6–8] and native oxide films[9] has been studied previously. At elevated temperatures and subatmospheric pressures, silicon oxide films decompose by the interfacial reactions $Si+SiO_2 \rightarrow 2SiO(g)$.[10] The decomposition of the oxide film is spatially inhomogeneous: decomposition starts locally and proceeds laterally as the reaction proceeds at the void perimeter. The clean surface of the void is lower than the oxide/Si interface due to bulk Si consumption.[5,7] This mechanism leaves the oxide areas between the voids unperturbed, i.e., there is no oxide film thinning observed. For thermal oxide films of 50–500 Å thick,[3,4] it has been suggested that the voids are nucleated at defect sites. The void size grows linearly with time for diameters in the range 2–80 μm, but the number of voids is nearly unchanged with continued annealing at $T \geq 1000$ °C. This behavior was attributed to the perimeter interfacial SiO reaction as the rate limiting step in void development.

In previous scanning tunneling microscopy (STM) studies of oxide films formed by room temperature (RT) O_2 adsorption,[7,8] much smaller voids were observed on annealing and again no new voids were observed once desorption was initiated. However, modeling of the void size evolution with annealing indicated that the production of a mobile Si monomer is the rate limiting step in void development.

In this letter, we present the results of void formation on ultrathin thermal oxide films (~1 nm thick). A mechanism for void formation is observed where the number of voids (void density) increases with annealing and existing voids continue to grow marginally. These results are consistent with Si-monomer formation as a rate limiting step in void development.

The experiments were performed in a multiple-chamber ultrahigh vacuum (UHV) system equipped with a scanning tunneling/atomic force microscope[11] and a monochromatic x-ray photoelectron spectroscopy (XPS) system.[12] The samples were *P*-doped *n*-type Si(100) (ρ=0.1 Ω cm). The surfaces were cleaned by standard resistive heating methods resulting in well-ordered Si(100)−(2×1) reconstruction with very low defect density (<2%). Surface temperature was monitored by calibrated optical pyrometry. Chemical analysis of the surface by XPS indicated that impurities were below the detectable limits (<1%). The ultrathin (~1 nm) oxide films were formed thermally by exposure to 5×10^{-5} Torr O_2 at 650 °C for 90 s. The thickness of the oxide film was determined by XPS.[13,14] The morphological evolution of the voids after thermal annealing in UHV was measured by STM.

After the oxide was grown, no long-range atomic structure can be resolved by STM. In contrast to the case of RT O_2 adsorption,[7,8] steps and terraces which correspond to the underlying Si(100) substrate are not observed.

Figure 1 is a series of STM images showing the sequence of void formation when the ultrathin thermal oxide is annealed at 750 °C for different durations. Before the voids start to overlap [Fig. 1(a)], the sizes of the voids observed here (~300–400 nm^2) are much smaller than those observed on thicker thermal oxide films (≥3 μm^2)[3,4] but larger than those observed on ultrathin oxides grown by the means of RT O_2 adsorption (≤40 nm^2)[6–8] at comparable annealing temperatures. The depth of the voids in the region depicted in Fig. 1(a) is estimated to be 1.2 nm by STM and is uncertain due to the differences in the tip–Si and tip–oxide tunneling barriers.

It is apparent from the STM image sequence that the void density increases with annealing duration. Also, before the void density increases to the point that the voids start to coalesce [Fig. 1(c)], the void size initially increases and appears to reach a limiting size. From such STM images taken before the voids started to strongly overlap (i.e., individual voids can still be distinguished), we measured the void density [Fig. 2 (●)] and averaged void size [Fig. 2 (○] as func-

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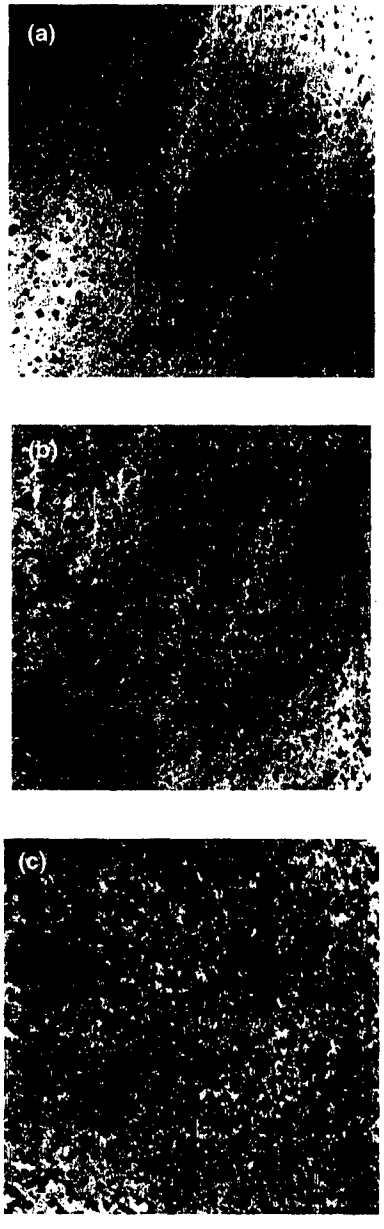

FIG. 1. Evolution of oxide void formation after annealing at 750 °C for (a) 30, (b), 90, and (c) 120 s durations. Scan area of all images is 500 nm×500 nm; sample bias +3 V.

tions ofannealing duration to reveal this dependence. These results are in contrast to the void formation observations on thicker thermal oxide films where void density was constant and the void size increased linearly with annealing duration at $T>1000$ °C. A similar observation of constant void density was also reported for the RT ultrathin oxides.[7,8] We observe an increase in void density in the ultrathin thermal oxide during annealing; our results suggest that the density of defects which gives rise to void formation in ultrathin Si-oxide films also increases with temperature. We also observe a decrease in the rate of void growth (area) which suggests that the rate of void growth is affected by the UHV annealing process while the rate of void nucleation is not.

The difference in void formation behavior between thick and ultrathin Si-oxide films is intriguing. Under the growth conditions here, the SiO formation reaction occurs at the oxide/Si interface. For thicker oxide films, initiation of the

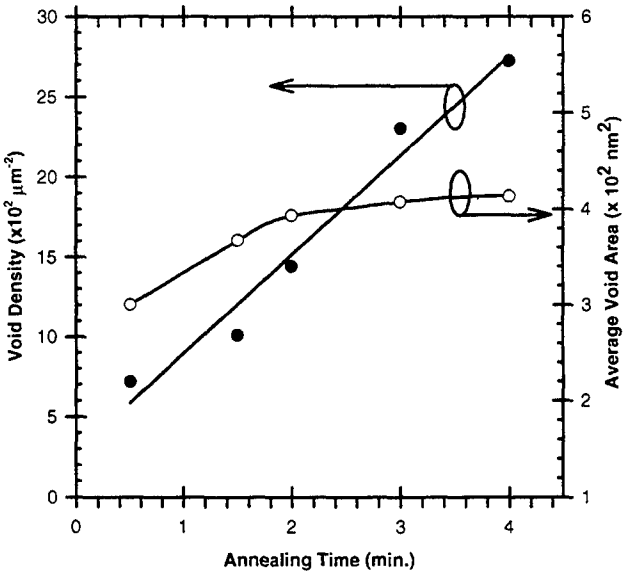

FIG. 2. Void number density (●) increases linearly with annealing duration. A marginal increase in void size (○) is observed with annealing.

voids results from SiO formation at the interface which must diffuse through the oxide film to escape from the interface. Assuming that defect sites in the thicker oxide films or at the oxide/Si interface provide efficient pathways for SiO liberation, the voids would prefer to open about these oxide defect sites. The spatial resolution limitations of the electron microscopy methods employed in the earlier studies[3–5] and the SiO diffusion processes are likely the cause for the failure of the detection of the voids of the size reported here, although the existence of "microvoids" (smaller than those reported here) was supported from positron-annihilation experiments.[4]

In ultrathin Si-oxide films, the SiO formed at the interface is readily liberated and does not require oxide defect pathways. Thus it is reasonable that void formation would proceed randomly throughout the oxide film and the void density would continue to increase, as is observed here. In previous studies of void formation on ultrathin oxides formed by room temperature O_2 adsorption,[7,8] it was concluded that the production of a mobile monomer (which then diffused to the void perimeter to react with oxide to form SiO) is the only rate limiting step. The diffusion of Si monomer on ideal Si(100) surfaces has been examined experimentally[15] and in theoretical treatments[16–18] where activation energies of diffusion <1 eV have been reported. Although the void base surface morphology here is considerably more complicated than the ideal Si(100) surfaces studied, we also assume that the monomer diffusion to the perimeter is facile.

The increase in void density with annealing duration observed concomitantly with marginal void growth under the conditions employed here is also consistent with the formation of a Si monomer as the rate limiting step in void development.[7,8] Experimental evidence for the activation energy for mobile Si-monomer formation is lacking, but estimates of ~3.5–4 eV are consistent with Si adatom bond scission (3 eV) and bulk Si bond scission (4.3 eV).[17,18] Re-

cently, we calculated the activation energy of Si-monomer formation to be in the range of 3.2–4 eV using first-principles density functional theory.[19] As experimental results indicate that the activation energy for SiO formation is 3.2–3.6 eV,[6,8] the observed marginal increase in void formation here is consistent with this estimate. Thus, at the temperature employed here (750 °C), the creation of the Si monomer *and* the SiO production competes kinetically in the void formation process.

We conclude that, on the ultrathin thermal oxide film, voids form randomly during annealing. Before the voids start to overlap, the void density continues to increase but the void size increases marginally, in contrast to void formation on thickener oxides. The difference in the behavior of void formation between the ultrathin oxide and thicker oxides is explained by the ready liberation of SiO through the ultrathin oxide. The void enlargement is limited by the creation of Si monomers. However, Si monomer creation *and* SiO production compete kinetically in the void formation process.

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Appendix D

Controlled growth of SiO_2 tunnel barrier and crystalline Si quantum wells for Si resonant tunneling diodes, *Journal of Applied Physics* 81 (1997) 6415.

Controlled growth of SiO_2 tunnel barrier and crystalline Si quantum wells for Si resonant tunneling diodes

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Two methods for producing Si-oxide barriers upon which crystalline Si layers can be grown are presented. One method entails oxide island nucleation on a clean vicinal Si(001) surface. The second method makes use of void formation in ultrathin oxides on the Si(100) surface at elevated temperatures. Either method results in an oxide barrier which is porous and the exposed Si within these pores can serve as a way to seed *c*-Si overgrowth. We demonstrate that it is feasible to grow crystalline Si overlayers on top of such porous oxide barriers, while on the continuous Si-oxide surface, only amorphous or nanocrystalline Si layer overgrowth can be achieved. The controlled oxide growth and Si overgrowth on the oxide can find possible applications in Si-based resonant tunneling devices, optoelectronics, and other Si-based nanoelectronics. © *1997 American Institute of Physics.* [S0021-8979(97)08509-5]

I. INTRODUCTION

The best Si-based resonant tunneling diodes (RTDs) obtained to date have been produced by epitaxial release and placement of III–V heterostructures onto Si,[1] but the process incompatibility with mainstream Si technology limits their commercial applications. Epitaxial growth of III–V and Si/SiGe RTDs directly onto Si for electron tunneling suffers a similar process incompatibility as well as a low peak-to-valley current ratio (PVR).[2–4] Other candidate barrier materials for Si resonant tunneling, such as CaF_2,[5,6] SiO_2,[7] ZnS,[8] and ternaries based on Mg, Se, and SiGeC,[9] could provide useful conduction band offsets and corresponding high PVRs for room temperature circuit operation. Of these, SiO_2 is highly desirable as an RTD barrier material as its process capabilities and manufacturability are well established and used in current Si production lines.

One of the key issues in the construction of silicon based resonant tunneling devices with silicon oxide as the tunneling barrier is how to produce a crystalline Si quantum well (QW) layer over the Si-oxide tunneling barrier. It has been shown that a Si overlayer grown on an amorphous Si-oxide can be amorphous or microcrystalline.[10] One way to grow crystalline Si QW layers upon an ultrathin silicon oxide barriers is to create nanometer-size holes (voids) in the oxide film. The crystalline silicon exposed by these holes acts as "seeds" for nucleation of crystalline Si overlayers. It is important in this case that the void dimensions are small relative to the electron wavelength so that the tunneling potential barrier remains essentially continuous to the impinging electron.[11] In this article, we report two methods which can be used to produce such tunneling barriers.

The first barrier growth method entails the use of the kinetic competition between nucleation of SiO_2 islands and the formation of gas phase SiO (etching of the Si surface) within the temperature-pressure phase space. By controlling the temperature and the O_2 pressure, the size and density of the oxide islands can be controlled while a clean crystalline Si surface exists between the islands. The second barrier growth method starts with a continuous ultrathin oxide film grown on an atomically clean Si(100) surface; voids are formed in the oxide film through the controlled production of volatile SiO. The desorption of the ultrathin oxide film is inhomogeneous and we find that the density and size of the voids are functions of the annealing temperature and annealing time under ultrahigh vacuum (UHV) conditions.[12]

II. EXPERIMENT

The experiments were performed in a multiple-chamber UHV system equipped with an atomic force/scanning tunneling microscope [OMICRON UHV atomic force microscope/scanning tunneling microscope (AFM/STM)] and a monochromatic x-ray photoelectron spectroscopy (XPS) system (VG ESCALAB Mark II) shown in Fig. 1. The system is also equipped with low energy electron diffraction (LEED), Auger electron spectroscopy (AES), and thermal desorption spectroscopy (TDS) capability. The Si(100) sample (*P*-doped, $\rho = 0.1\ \Omega$ cm) is mounted onto a holder which is capable of transport and analysis throughout the surface analysis system.[13] The samples are transferred into the system through a loadlock to maintain UHV pressures (1×10^{-10} Torr) throughout the system. The loadlock is pumped initially by a Venturi pump from atmosphere to 1×10^{-3} Torr, and then by a turbo pump to 1×10^{-6} Torr. The sample is then delivered down to the transfer chamber which provides access to the XPS analytical chamber or the TDS/LEED/STM portion of the system. A combination of magnetic manipulators, wobble sticks, and sliding tracks enable sample transfer.

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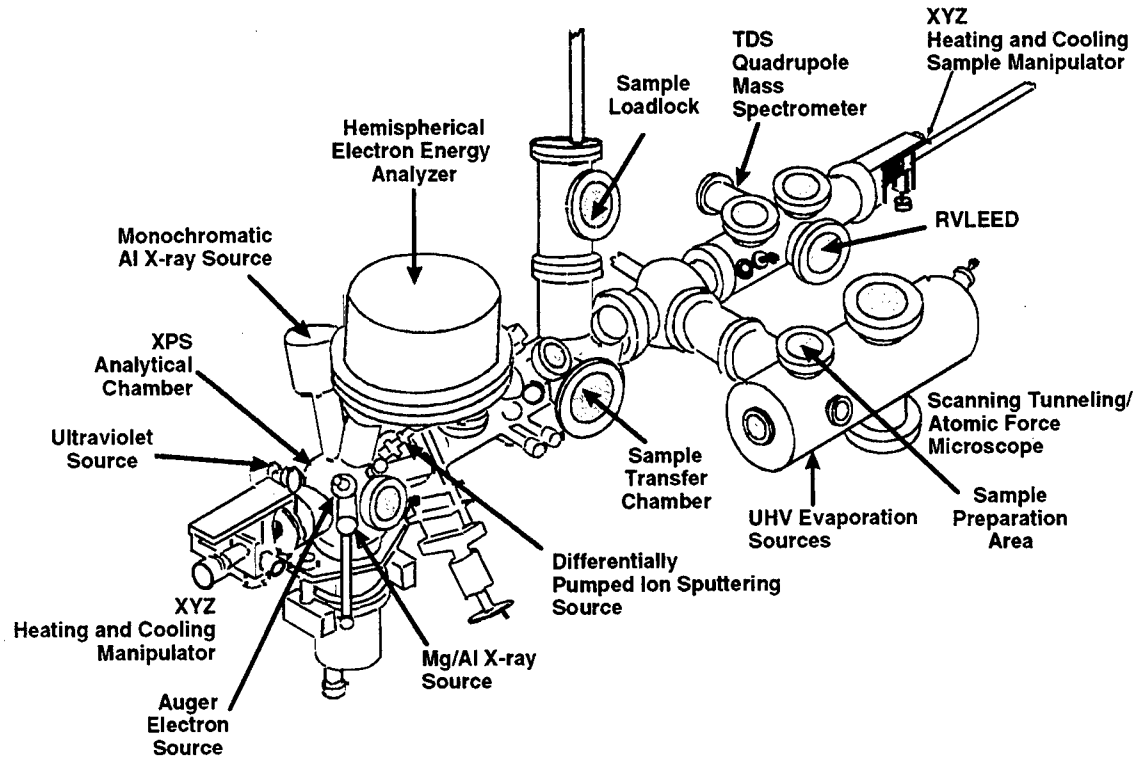


FIG. 1. Multitechnique surface analysis system used to study ultrathin oxides.

Two vicinal orientations were used in this study: 0.1° miscut (for oxide growth and void formation) and a 4° miscut toward the [011] direction (for oxide island nucleation). The surfaces are cleaned by standard resistive heating methods resulting in a well-ordered Si(100)−(2×1) reconstruction with a low defect density (<2%). Sample surfaces are prepared in a heated stage adjacent to the STM and quenched to room temperature prior to placement in the STM. Surface temperatures during the annealing process are monitored by a calibrated optical pyrometer with an accuracy estimated to be ±30 °C. Following STM examination of the prepared surface, XPS indicated that surface impurities were below detectable limits (<1 at. %). The ultrathin (~ 1 nm) oxide films are formed thermally by exposure to 5×10^{-5} Torr O_2 (research grade) at 650 °C for 90 S. The thickness of the oxide film was determined by XPS measurements. The morphological evolution of the voids after thermal annealing in UHV was measured by STM.

In the Si overgrowth studies, Si is deposited onto the surface by using an OMICRON EFM-3 evaporator equipped with water cooling. The Si source consists of an intrinsic Si rod 1.5 mm in diameter. The tip of the Si rod is melted by electron bombardment from a hot W-filament which results in a high Si vapor pressure thus producing the required Si flux. Deposition rates range from 1–1.5 Å/min and the pressure of the system is kept below 1×10^{-9} Torr during Si evaporation.

III. RESULTS AND DISCUSSION

A. Oxide island nucleation on the vicinal Si(100) surface

When O_2 reacts with clean silicon surfaces, two processes take place: (a) growth of a SiO_2 film via the reaction $Si+O_2\rightarrow SiO_2$ at low temperatures and high oxygen partial pressures; and (b) formation of volatile SiO via reaction $2Si+O_2\rightarrow 2SiO(g)$, which leads to etching of the surface at high temperatures and low oxygen partial pressures.[14]

To achieve the required control of oxide island size and density, we have examined the SiO_2/SiO phase space shown in Fig. 2. A well known "critical line" which separates the SiO_2 growth and etching of the Si surface in O_2 pressure-

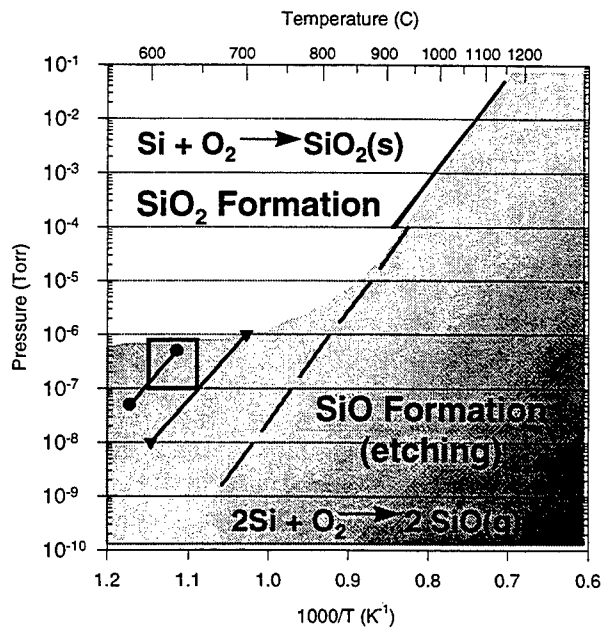


FIG. 2. Pressure-temperature phase diagram for O_2 interaction with a Si surface. The boxed region corresponds to the oxide-island nucleation region reported here. – – – Ref. 14; ——— Ref. 15; ▼–▼ Ref. 16; ●–● Ref. 17.

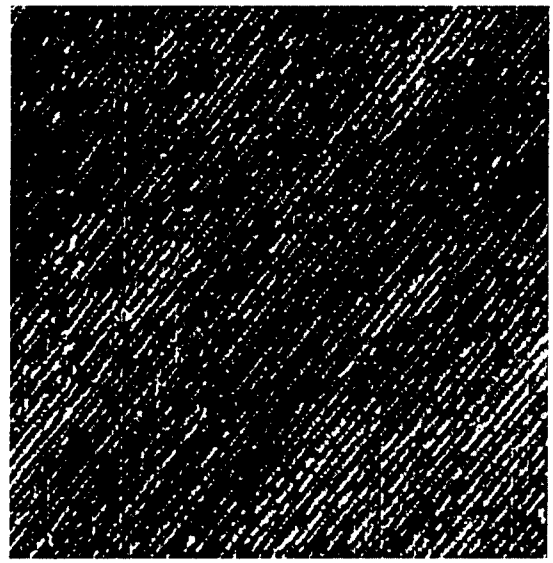
substrate temperature phase diagram has been established using the LEED method[14] and emissivity changes and/or optical inspection.[15] By combining these early studies and the results of more recent studies[16–18] of these processes, a "critical curve" is established as shown in Fig. 2. Within the gray region, the reaction of Si and O_2 produces volatile $SiO(g)$, while within the white region the reaction results in SiO_2 growth. We note that it has been suggested that the deviation of the curve from the original line might be due to experimental artifacts.[19] However, the recent STM and low energy electron microscopy (LEEM) studies[17,18] and our work within the SiO_2–SiO phase space indicates that the deviation is real.

In the vicinity of the critical curve, etching of the Si surface as well as oxide island nucleation are expected.[15,16] However, within this etching to nucleation transition region, the oxide nucleation rate depends on the surface miscut angle. On the nominally flat Si(100) surface, nucleation sites are difficult to detect.[17,18] On the Si(100) surface with a small miscut angle, oxide nucleation sites start to form after prolonged oxygen exposure and can be detected.[17]

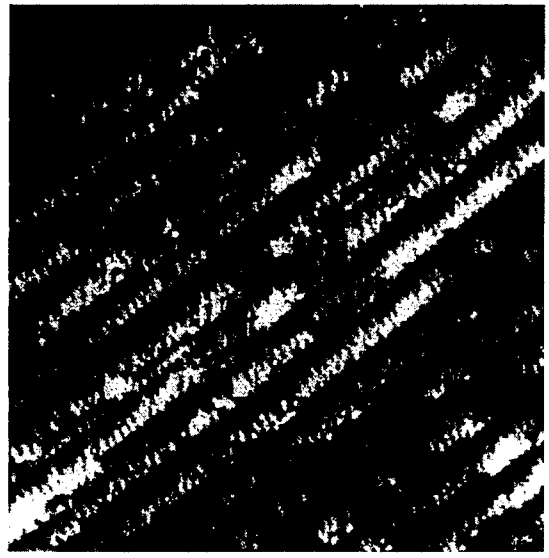
In our experiment, the Si(100) surface with a 4° miscut towards [011] was used. This surface has high step density, with evenly spaced double B-type (D_B) steps of 2.8 Å height. Dimer rows on the terraces are perpendicular to the step edges. The high step density is expected to increase the nucleation rate of oxide islands, which can avoid a long exposure time needed to achieve high oxide island density and island size. Figure 3(a) shows a typical large scale STM image of the clean surface and a smaller scan [Fig. 3(b)] with dimer row resolution. After the low defect density surface is obtained, it is exposed to various oxygen pressures at different substrate temperatures in the vicinity of the critical curve in the pressure-temperature phase diagram for island nucleation outlined in Fig. 2.

Figure 4 shows a series of STM images of the vicinal Si(100) surface exposed to 1×10^{-7} Torr O_2 at 600 °C as a function of exposure time. Figure 4(a) is a 500 nm ×500 nm area of the surface after it has been exposed to O_2 for 5 min (30 L, 1 $L=1\times10^{-6}$ Torr×s); small oxide nucleation centers (~ 2–5 nm diameter) have formed. Figure 4(b) is a higher resolution scan (50 nm×50 nm) of the same surface where the oxide nucleation centers (bright areas) are evident and the steps are clearly visible but with a smaller terrace width than that of the original 4° miscut surface. On Si(100) surfaces with small miscut angles towards the [011] direction (i.e., where A- and B-type steps are observed), the oxygen induced etching happens preferentially at B-type steps, causing the retraction of B-type steps, and the oxide nucleation centers act as pinning centers for step motion.[16,18] Thus, the surface etching proceeds in the step-flow mode.

On the 4° miscut Si(100) surface, where step edges are double B-type (D_B), oxide nucleation promotes etching in the vertical direction, instead of through B-type step edge etching. Thus, even in the very early stage of the oxide island nucleation, the local terrace width is smaller than the original miscut terrace, since the vertical etching will create a bigger local miscut angle. Figures 4(c) and 4(d) show the 4° miscut surface after O_2 exposure at the same conditions for 10 and 15 min, respectively. It is evident that the sizes of the oxide islands become bigger.



(a)



(b)

FIG. 3. Clean vicinal Si(100) surface. 4° miscut towards [011]: (a) 200 nm×200 nm; (b) 53 nm×53 nm. Sample bias is −2 V for both images.

Figure 5 shows the evolution of the average island size [Fig. 5(a)] and the oxide island density [Fig. 5(b)] as a function of exposure time to the oxygen (1×10^{-7} Torr, 600 °C). Initially, the average size of an oxide island increases with exposure, and then saturates at higher exposures. For the island density, a rapid increase is observed in the lower dose region which may be a result of the competition between two processes, viz., solid phase SiO_2 formation and gas phase SiO formation, where SiO_2 formation dominates resulting in a large oxide island density. However in the context of controlled island growth, the more important feature of the island density-exposure time relationship is the observed density saturation at the time where the island size also reaches saturation (~15 min). The observation of island density saturation is consistent with the oxide nucleation being

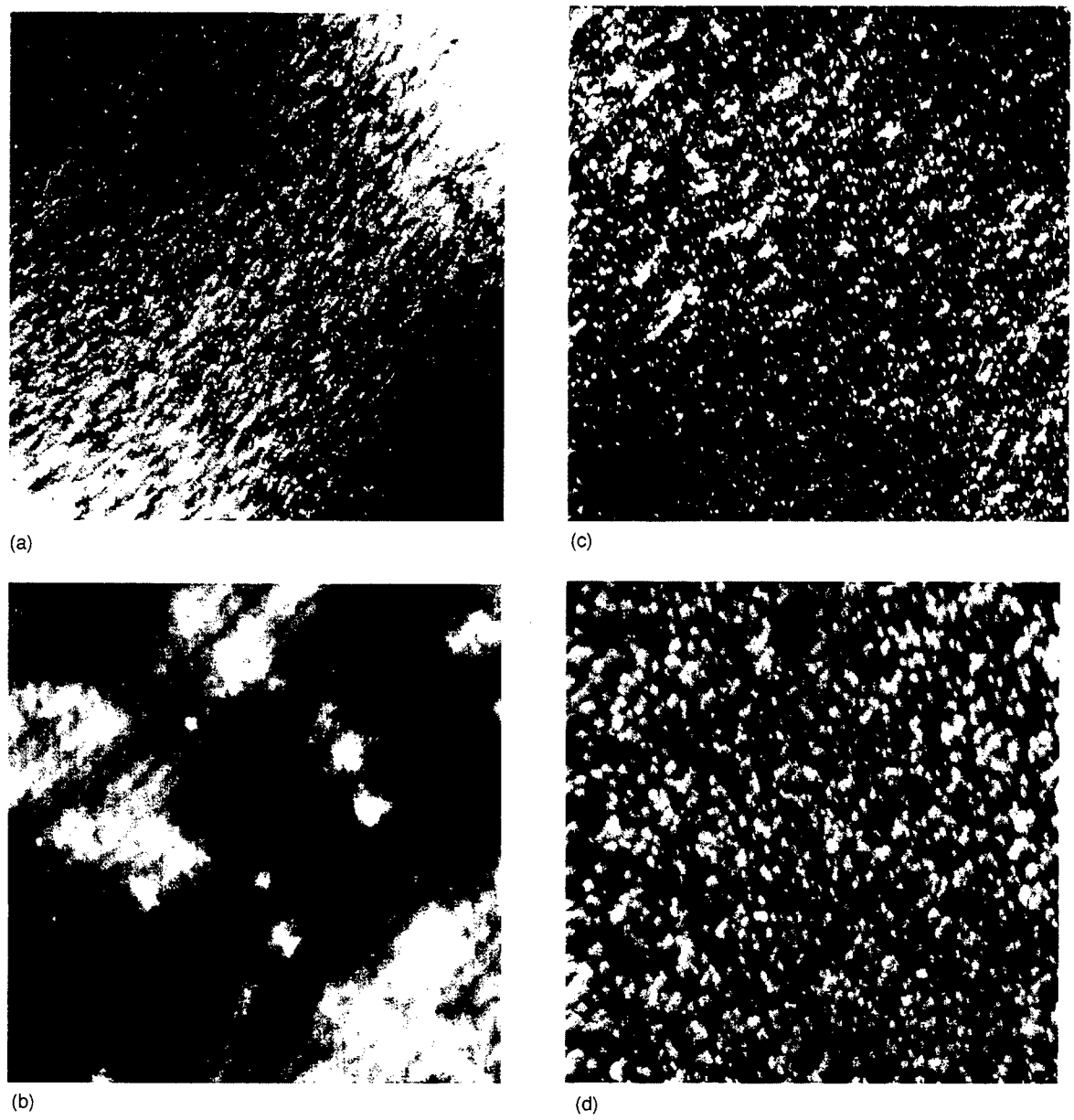


FIG. 4. Evolution of the vicinal surface after exposure to 1×10^{-7} Torr O_2 at 600 °C. (a) and (b) 5 min; (c) 10 min; (d) 15 min. The scan area is 500 nm×500 nm for (a), (c), and (d), 50 nm×50 nm for (b). The sample bias is +3 V for all images.

strongly suppressed at a high O_2 dose on flat Si(100) surfaces observed by Seiple *et al.*, albeit at a much higher dose (~200 L).[20,21] The fact that both oxide island size and density saturate at higher doses makes it possible to obtain the desired island size and density repeatedly for controlled oxide barrier growth.

The density of oxide islands is also sensitive to the oxygen partial pressure. Figure 6 shows the surface after being exposed to 7×10^{-8} Torr O_2 at 600 °C for 15 min where it is evident that the island density is much lower than that shown in Fig. 4(d). Thus the oxide island density can also be controlled by varying O_2 pressure.

Figure 7 shows a three-dimensional STM image of these oxide islands. The oxide layer is on top of the cone shape structures preventing the underlying Si from being etched.[15,20] However, oxygen keeps etching the surrounding unshielded region. This also provides an effective way to create Si pillars with regular size when the oxide nucleation and etching reach equilibrium. Such structures may also have possible applications in Si nanoelectronics.

B. Void formation on ultrathin thermal oxide

Void formation on thermally grown oxide films[22–24] and ultrathin oxide films formed by room temperature O_2 adsorption[25–27] is well known. At elevated temperatures and subatmospheric pressures, silicon oxide films decompose by the interfacial reaction $Si+SiO_2\rightarrow 2SiO(g)$ thus producing voids in the film.[14] We have examined the thermal stability of continuous oxide films (as determined by STM images) under vacuum and have been unable to detect the presence of voids in these films after 30 min of annealing at 600 °C.

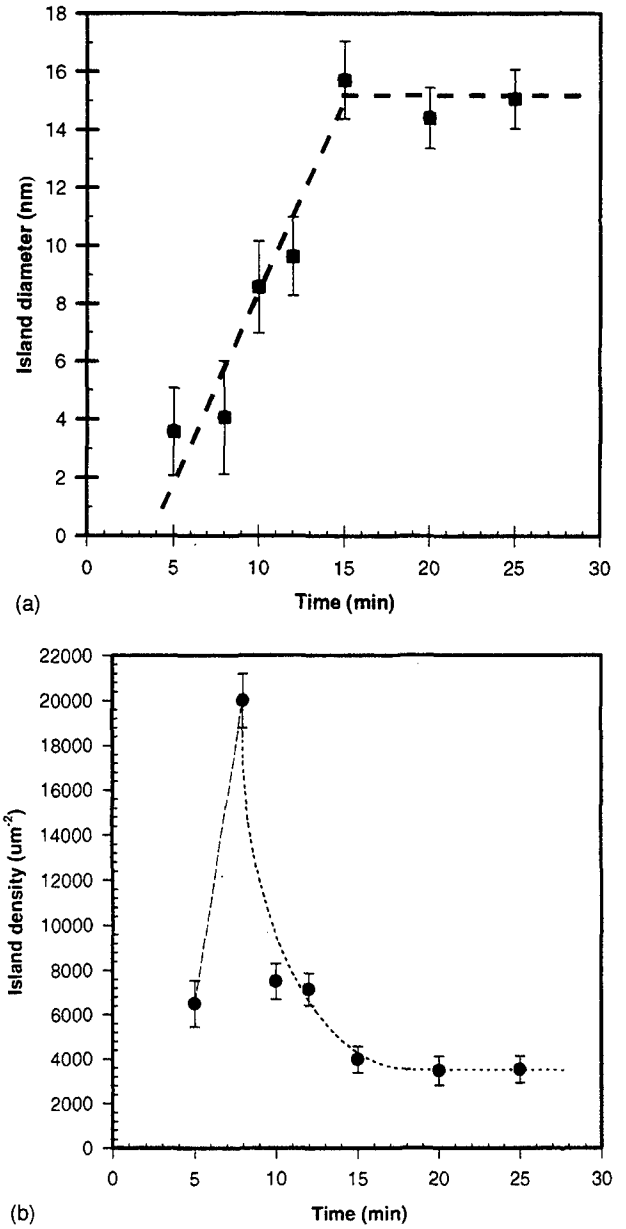


FIG. 5. (a) Average oxide island size as a function of exposure time; (b) oxide island density as a function of exposure time.

Higher annealing temperatures (~700 °C) can lead to void formation in shorter annealing durations (~5 min).

After a void is initiated, enlargement occurs through a three-step mechanism:[26,27] (a) Si-monomers are created on the exposed Si surface, (b) facile Si-monomers diffuse to the void perimeter where they (c) react with the oxide to form volatile SiO, as illustrated in Fig. 8. The decomposition of the oxide film is spatially inhomogeneous: decomposition starts locally and proceeds laterally as the reaction proceeds at the void perimeter. The clean surface of the void is lower than the oxide/Si interface due to the bulk Si consumption (i.e., etching).[26,27] This mechanism leaves the oxide areas between the voids unperturbed, i.e., there is no oxide film thinning observed.

For thermal oxide films of 50 to 500 Å thick[22,23] it has been suggested that the voids are nucleated at defect sites

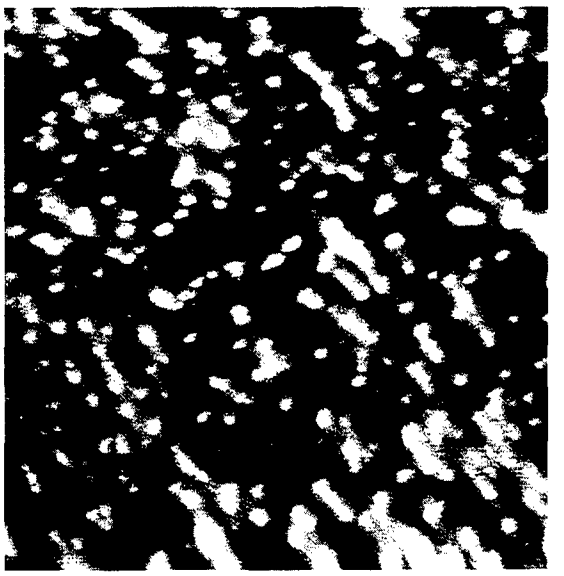


FIG. 6. A 4° off vicinal Si(100) surface has been exposed to 7 × 10^{-8} Torr O_2 at 600 °C for 15 min. Scan area is 500 nm×500 nm. Sample bias is + 3 V.

because the void number density is observed to remain constant as a function of annealing duration. The sizes of the voids observed on the thick thermal oxides are in the μm-range[21–23]—too large for use as a tunneling barrier. Such oxide films are also too thick for resonant tunneling devices which need an oxide thickness resulting in direct tunneling (<35 Å). The void size grows linearly with time for diameters in the range of 2–80 μm, but the number of voids is nearly unchanged with continued annealing at $T \geqslant 1000$ °C. This behavior was attributed to the perimeter interfacial SiO reaction as the rate limiting step in void development. Since the number density of the voids in thick thermal oxides is constant and the void size increases linearly during annealing in this case, control of the number density of voids for crystalline Si overlayers growth is not possible.

In contrast to the thick oxide case, void formation on ultrathin thermal oxides is controllable. After growth of a ~10 Å thick oxide on atomically clean Si(100) surface (by exposure to 5×10^{-5} Torr O_2 at 650 °C), the oxide is annealed at 750 °C in UHV. Figure 9 is a series of STM images

FIG. 7. Three-dimensional STM image of the oxide islands and the surface etching effect. Scan area is 25 nm×25 nm. Sample bias is + 3 V.

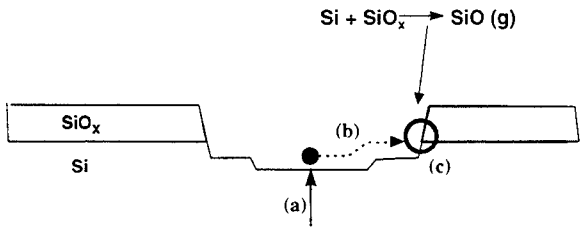


FIG. 8. Three-step mechanism schematic of void formation in silicon oxide. (a) Mobile Si-monomer formation, (b) Si-monomer diffusion, and (c) SiO formation. Process (b) is considered to be facile.

showing the sequence of void formation when the ultrathin oxide is annealed for different durations. Before the voids start to overlap, the sizes of the voids observed here ($\sim$300–400 nm^2) are much smaller than that observed on thicker thermal oxide films ($\geq 3\ \mu$m^2).[22,23] In these STM images, we clearly observe that the void number density increases with annealing duration. Also, before the void density increases to the point that the voids start to coalesce [Fig. 9(c)], the void size increases marginally. We have also found in subsequent annealing experiments (not shown here) that the observed void morphology is stable to at least 650 °C for annealing durations of 30 min within STM detection limits.

From such STM images, we measured the void density [Fig. 9(d)] and average void size as functions of annealing duration to reveal this dependence. These results are in contrast to the void formation observations on thicker thermal oxide films where void density was constant and the void size increased linearly with annealing duration at $T > 1000$ °C.[22–24]

The reasons for the differences in void formation behavior in thick thermal oxide and ultrathin thermal oxide have

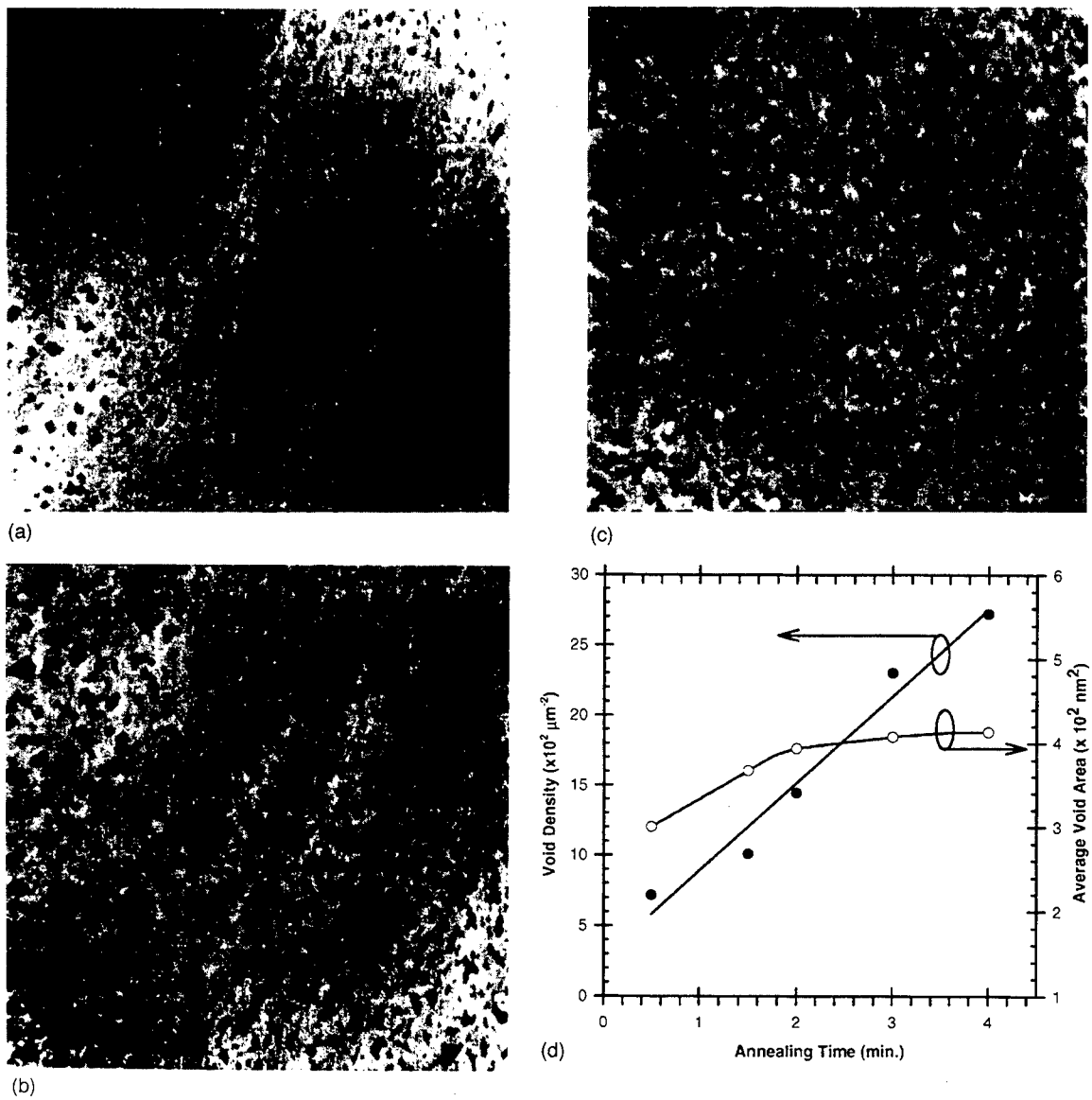


FIG. 9. Evolution of oxide morphology after annealing at 750 °C for (a) 30 s, (b) 90 s, (c) 120 s duration. Scan area is 500 nm×500 nm for all images. Sample bias + 3 V. (d) Void number density (filled circles) increases linearly with annealing duration. A marginal increase in void size (open circles) is observed with annealing duration.

FIG. 10. Clean Si surface within an oxide void.

been explained elsewhere.[12] Under the growth conditions employed here, the SiO formation reaction occurs at the oxide/Si interface. For thicker oxide films, initiation of the voids results from interfacial SiO formation and subsequent diffusion of SiO through the oxide film to be liberated. For the ultrathin films, SiO liberation proceeds unimpeded.

We have also recently examined the energetics which explain the coexistence of void size enlargement and void number density increase during annealing using first-principles density functional methods.[28] We find that the calculated activation energy of Si-monomer formation to be in the range of 3.6–4.6 eV. Experimental results indicate that the activation energy for SiO formation is 3.5–4.3 eV.[25] The observed marginal increase in void size and the linear increase in number density observed here is consistent with the activation energies of the two processes (Si-monomer formation and SiO formation) being essentially indistinguishable. That is, both reactions channels kinetically compete in the void enlargement process. Of course, the rate limiting step for void *initiation* is SiO formation, as it is the only reaction involved.

After void initiation has occurred and the Si surface within the void is exposed, the three-step process involved with void enlargement can be considered, viz., (a) mobile Si-monomer formation, (b) Si monomer diffusion, and (c) SiO formation. The exposed Si surface within a void is shown in Fig. 10. It may be seen that this surface presents a number of elevated features (possibly residual oxide islands) amongst flat terraces. Steps are observed to separate the flat terrace regions and step bunching is also observed near some of the elevated features. This observed surface morphology would require a mobile Si-monomer to diffuse in an "upstep" direction over the terraces, as well as potential interactions with the elevated features, in order to react with SiO_x present at the void perimeter. Thus, one may anticipate some energetic barriers to monomer diffusion. However, diffusion of Si-monomers on the ideal Si(100) surface has been shown to be facile (<1 eV diffusion activation energies).[29] Although the surface shown in Fig. 10 is far from ideal, we also assume the Si-monomer diffusion over the step features is also facile. Thus we consider only the monomer and SiO formation processes in the void formation.[26,27]

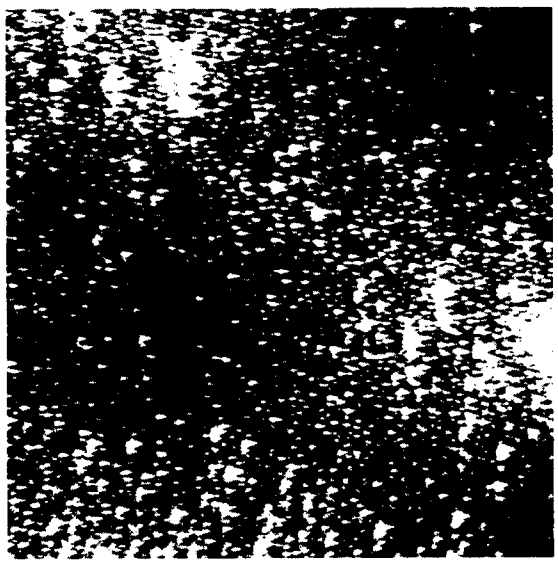
If the activation energy for SiO formation is much larger than that of Si-monomer formation, then one would not expect to observe an increase of void density with annealing duration and void enlargement would be observed. Conversely, if the activation energy of Si-monomer formation is much larger than that of SiO formation, an increase in void number density is expected and the size of the voids would increase at a lower rate. Therefore, to explain the increase of both void number density and void size during annealing as observed here, the activation energy of SiO formation and that of Si-monomer formation must be comparable, which is consistent with our first-principles cluster calculations.[28]

Since we observe that both void size and void density increase during annealing of ultrathin oxide films, it is possible to control the void size and number density in the ultrathin oxide film so that the surfaces within the voids can serve as seeds for the overgrowth of crystalline Si. By controlling the size and number of voids in the oxide, a tunneling barrier for Si-based resonant tunneling devices may be produced. We note that this is also a promising way to produce a new kind of silicon-on-insulator (SOI) structure, which the silicon layer on top of the insulator (oxide) is crystalline. This could improve the quality of the SOI structure and the performance of devices built in the SOI structure.

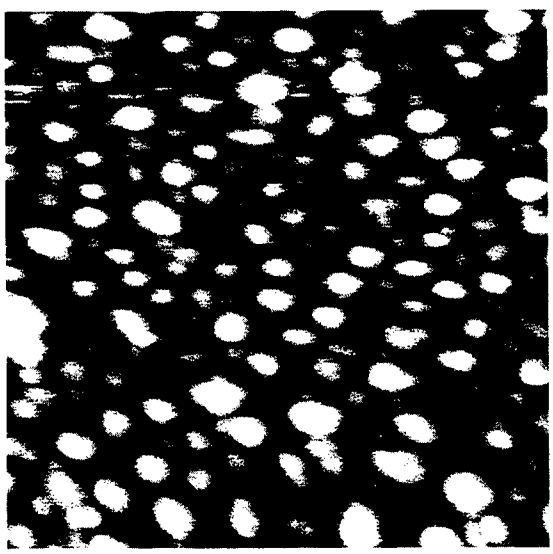
C. Si overgrowth on the oxide barriers

As shown above, void formation in oxide films can be controlled by control of annealing temperatures and duration in vacuum. Stable continuous oxide films are observed for sample temperatures near 600 °C for durations of at least 30 min. Deposition of Si on such a continuous ultrathin oxide film at elevated temperatures can result in the formation of polycrystalline silicon, as shown in Fig. 11. This Si film was deposited at 600 °C and has a film thickness of ~40 Å. The size of these "nanocrystals" is ~100 Å in diameter and a height of ~30 Å. A perspective view of these features is presented in Fig. 11(c). At a higher surface temperature (630 °C), the nanocrystals grow in size to form a polycrystalline grain structure (Fig. 12), as expected from the enhanced diffusivity of Si atoms at the higher temperatures. An edge delineated STM image of this granular structure is shown in Fig. 12(c) where the boundaries between the nanocrystals are clearly visible. The angles between these boundaries are ~60° and ~120° which reflect the symmetry of (111) facets of Si.

This result demonstrates that the ultrathin (10 Å) continuous amorphous oxide layer appears to be effective in precluding single-crystal Si overgrowth. Previous studies have examined the potential of epitaxial growth upon single crystal substrates where thin amorphous oxides are present.[30] In these studies, the observation of preferential orientation of layers over an amorphous oxide was explained by "long range ordering effects" through the amorphous layer. Although the results here do not directly refute such explana-



(a)



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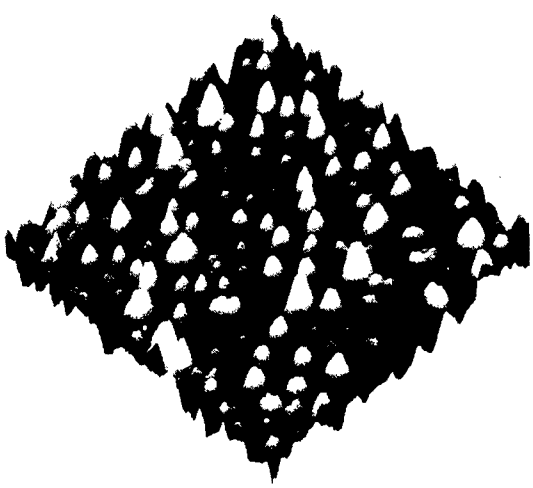
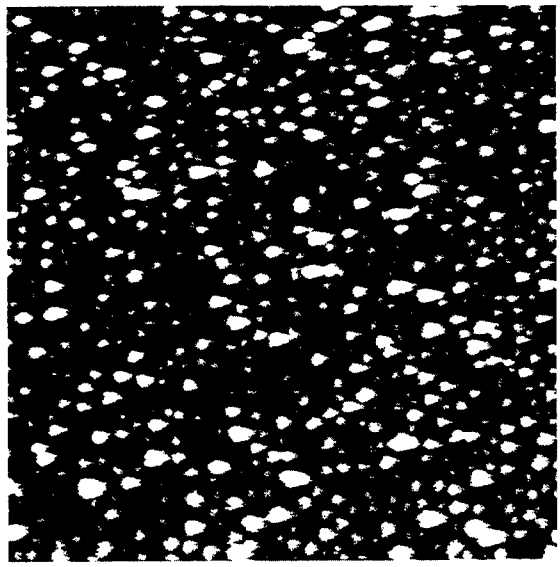
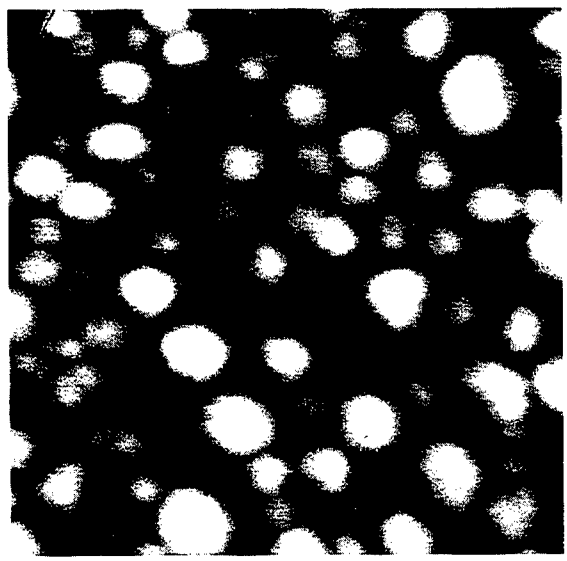


(c)

FIG. 11. (a) 500 nm × 500 nm STM image of Si nanocrystals grown on ultrathin oxide at 600 °C. (b) 100 nm × 100 nm region in (a). (c) perspective view of the nanocrystal structure.



(a)



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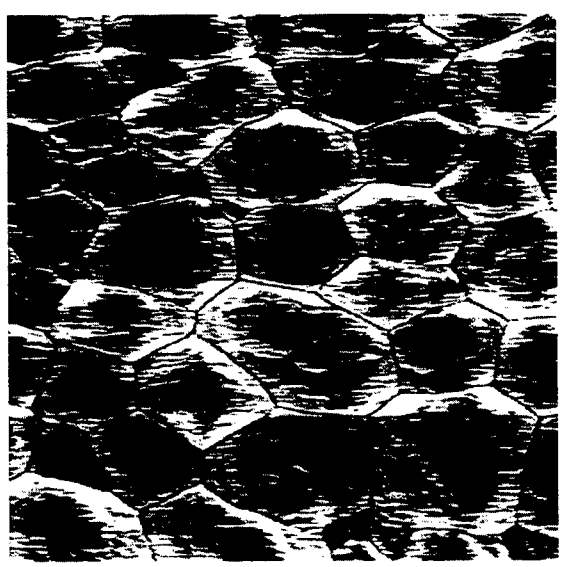

(c)

FIG. 12. (a) 500 nm×500 nm image of Si nanocrystals grown on ultrathin oxide at 630 °C. (b) 100 nm×100 nm image in (a). (c) 50 nm×50 nm edge delineated STM image showing the grain boundaries.

(a)

(b)

FIG. 13. (a) 200 nm×200 nm STM image after Si overgrowth, (b) 20 nm×20 nm region in (a). The Si(100)−(2×1) reconstruction is observed indicating crystalline overgrowth.

tions, we note that the presence of voids in thin oxide films whose size is below our detection limits could be possible.[26,27] We have observed polycrystalline overgrowth (not shown here) under conditions where voids with detectable sizes are deliberately introduced with a density so as to facilitate the observed poly-Si growth.

Finally we examine the feasibility of the growth of a crystalline Si overlayer on top of the porous oxide barriers. The porous oxide employed here is produced by using the void formation method described previously. After the growth of ~10 Å continuous oxide, the film is annealed at 750 °C for 3 min in UHV to create voids throughout the film. Deposition of a ~60 Å Si film on this porous oxide at 600 °C (where the void morphology remains thermally stable) results in the production of an ordered, single crystal Si layer, as seen in Fig. 13. In Fig. 13(a), flat domains can be seen on the surface with Si overlayers. A higher spatial resolution image on the flat domains is shown in Fig. 13(b), where the Si(100)−(2×1) dimer reconstruction is evident.

This result verifies the feasibility of the production of an ordered Si layer over a porous Si-oxide barrier. Examination of the electrical properties of tunneling structures based on these growth methods, such as SiO_2/Si/SiO_2 RTDs, is currently in progress.

IV. SUMMARY

We have introduced two methods for controlled growth of Si-oxide barriers for Si based resonant tunneling devices. The first method utilizes the oxide island nucleation on a vicinal Si(100) surface. By controlling the O_2 pressure and substrate temperature, the desired oxide density and size suitable for Si overgrowth can be achieved. The second method starts with a continuous ultrathin thermal oxide film; voids are formed by inhomogeneous decomposition of the silicon oxide to expose the underlying clean crystalline Si surface. It is found that during the decomposition of ultrathin oxide, void number density increases linearly but void size increases marginally since both Si-monomer formation and SiO formation contribute to void enlargement. This phenomenon enables us to control the size and density of the voids by controlling the annealing temperature and time. Both methods form porous oxide networks where clean Si surfaces are exposed that can serve as seeds for the subsequent crystalline Si layer overgrowth. The surface of the overlayers has the (2×1) dimer reconstruction, which is the characteristic reconstruction on Si(100) surface.

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Appendix E

Energetics of void enlargement in thermally grown ultrathin Si-oxide on Si (001). Accepted for publication in *Surface Science Letters* (1997).

Energetics of Void Enlargement in Thermally Grown Ultrathin Si-Oxide on Si(001)

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ABSTRACT

The energetics of void enlargement in ultrathin Si-oxide is investigated by first principles density functional theory calculations and scanning tunneling microscopy. By calculating the energetics of Si monomer formation on Si(001) surface using cluster models containing up to 71 atoms, it is found that the activation energy of Si-monomer formation is within the range of SiO formation measured experimentally. This indicates that the rate limiting step of the void enlargement process by either Si monomer or SiO formation is indistinguishable. Scanning tunneling microscopy studies confirm this prediction where an increase of void size and an increase in void number density are concomitant.

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Keywords: surface, void formation, diffusion, Si monomer, density functional theory(DFT), scanning tunneling microscopy(STM)

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The continued reduction of integrated circuit size has created a revolution in many families of metal oxide semiconductor (MOS) technologies. One of the areas in MOS technology that receives great attention is ultrathin gate dielectric growth on silicon. Although many dielectric materials have been proposed, silicon oxide remains the primary choice for the gate dielectric. To realize a MOS device using ultrathin gate oxides, thermally stable oxide films are required.

As observed from previous experiments [1-8], ultrathin oxide films on Si decompose thermally during annealing, yielding volatile SiO(g) that results in void formation on the Si oxide surface. The decomposition of the oxide film is spatially inhomogeneous: decomposition starts locally and proceeds laterally as the reaction proceeds at the void perimeter. A reaction sequence for void formation has been proposed which includes Si-monomer formation, Si diffusion on the void surface, and SiO(g) formation[6,7]. However, which step controls the rate of void growth remains controversial. Rubloff et al. [2-4] concluded that the void growth is rate limited by the chemical reaction near the void periphery that yields volatile SiO for thick thermally grown oxides. In contrast, Johnson et al. [6,7] suggested that the creation of a mobile Si monomer within the void determines the rate of void growth for this oxides produced by room temperature O2 adsorption. Also in contrast to the results reported here, both of these groups reported an increase in void size without the observation of new void formation[8].

Previous experimental[9-11] and theoretical [12-19] studies on Si adatom diffusion on Si(001)(2x1) provided important fundamental understandings of the diffusion barrier and the diffusion path for a Si adatom. Although there are still discrepancies over the detailed diffusion path, all these studies agree that the preferred diffusion path is parallel to the Si dimer row orientation. The calculated activation energy[12-19] parallel to the dimer row is in the range of 0.24~0.76eV while the activation energy perpendicular to the dimer row is around 1eV. The experimentally determined diffusion barrier parallel to dimer row is 0.67(0.08eV[11]. For Si adatom diffusion over terraces and steps, the measured and calculated energy barriers are less than 2.4eV[9-12]. Thus, the Si monomer diffusion process on surface is considered to be relatively facile since the various energy barriers for Si adatom diffusion over terraces and steps is much smaller than, for example, the formation energy (3.5-4.3eV)[5] of SiO. Vacancy diffusion, with a measured energy of 1.7eV[20], is not considered in the reaction sequence as it is difficult to determine the corresponding reaction complex preceding SiO formation[7].

In this letter, we report combined theoretical and experimental studies on the dominant reaction that controls the rate of void growth. We find that the activation energy of

a Si monomer formation from a dimer is in the same range of SiO formation measured experimentally [5], indicating that both reactions are indistinguishable in affecting the rate of void growth. This prediction is confirmed by scanning tunneling microscopy (STM) studies which show that an increase in void size is accompanied by an increase in void number density. These results have important implications for the controlled growth of pinholes in ultrathin oxide films on the Si(001) surface.

The theoretical calculations were carried out using first-principles total energy molecular cluster approach (DMol)[21] within the local density approximation (LDA) to density functional theory. It has been shown that generalized gradient approximation (GGA) corrections to the standard LDA yield better agreement with experiment on, for example, the Si adatom binding energy on the Si surface[19]. In our calculation, the exchange and correlation energies are described in Ceperley-Alder[22] form of LDA and the gradient dependent functional for correlation energy[23] and exchange energy[24]. Other forms of local exchange-correlation functional[25] are also used. As expected, the calculated binding energy from LDA is about 0.6-0.8eV higher than that from the LDA-GGA results. A detailed comparison will be presented elsewhere[26]. The initial geometry of clean Si(001)(2x1) surface is taken from Tang et al. [27]. Cluster models containing up to 71 atoms as shown in Figure 1 are used to simulate the Si(001)(2x1) dimerized surface and Si monomer adsorption on Si(001). The first three layers of Si atoms are relaxed until the forces on movable atoms drop below 4.0 x 10-3 (Ry/a.u.) . Bulk Si dangling bonds are saturated using hydrogen atoms.

Since the oxide void enlargement consumes Si atoms at the surface, the continuous creation of mobile Si monomers is the essential step to enlarge an oxide void. It has been observed that the exposed surface of the void consists of dimer-based reconstruction[7] with extensive step structures resulting in a complicated surface morphology[8]. The formation of a mobile Si monomer entails Si-bond scission and reattachment at a nearby surface position so that the Si monomer can then readily diffuse in order to form SiO(g). Thus, the activation energy of a mobile Si monomer includes a formation energy of a mobile Si monomer and an energy to overcome the relevant surface diffusion barrier.

A way to calculate the activation energy of a Si monomer is to study the total energy surface as a function of monomer position (x,y) around the vacancy site from which the monomer is created[15]. For each possible diffusion path that connects potential binding sites for Si monomer, a maximum energy can be determined. The minimum energy among these maxima is then the minimum energy for diffusion. The activation energy of a mobile Si monomer then includes this minimum energy plus the energy required to reach the binding site from which the facile diffusion occurs. In this work, rather than calculating the energy

surface around the vacancy site, we derived the monomer activation energy simply based on the calculated binding energy of a monomer from a dimer structure and the assumption that the subsequent adsorption of a mobile Si monomer corresponds to a weakly bound species.

We started with a Si(001)(2x1) cluster model as shown in Fig.1(a) which contains three dimers in a dimer row. The calculated dimer bond energy which is defined as the energy gained from bulk terminated Si(001) to Si(001)(2x1) dimer surface is 1.66 eV/dimer. In comparison, previous theoretical calculations[28] gave results between 1.8~2.0eV. The smaller value of our results are mainly due to the use of the GGA correction to the LDA in the calculation. Consider a process that extracts a Si atom from the Si(001)(2x1) surface and moves it to a distance large enough to prohibit any interaction with the surface. The total energy required for such a process will then be the maximum energy (Emax) required to create a free Si atom. Readsorption of this free Si atom on the surface at a site (in the vicinity of a vacancy) which enables facile diffusion reduces the expended energy. A cluster shown in Fig.1(b) which has a vacancy in the dimer Si atom position can be used to study the energy needed for such process. The calculation is done by subtracting the total energy of the clean Si(001)(2x1) (Fig.1(a)) from the sum of the total energy of the surface with a single atom vacancy(Fig.1(b)) and the energy of a free Si atom. This yields Emax as 4.56eV.

The above monomer creation calculation assumes the Si atom be removed to a large distance from the surface. The actual process involves Si monomer diffusion on the surface, Si rebinding with a vacancy site and Si adsorption at other various surface sites. No matter what process is involved, the energy required to create a Si monomer is always less than Emax calculated above because even a weak subsequent bonding of the Si monomer with the substrate will release some energy. If, for example, the Si monomer adsorbs on the bridge site near a vacancy as shown in Fig. 1(c), we find that this process results in an adsorption energy of 2.91eV[29]. Thus Emax can be regarded as the upper limit of the activation energy of monomer formation. In practice, once a mobile Si monomer is created, the Si atom on the surface that was previously bonded with the bridge bonded monomer can also become a mobile monomer with a lower activation energy. Thus the upper limit of an average Si monomer formation activation energy should be somewhat less than 4.56eV.

We now consider the lower limit of the activation energy of Si monomer formation. Since the oxide void enlargement process requires a Si monomer which is mobile enough to diffuse to the void perimeter and form SiO(g), such Si monomers should be weakly bonded with the Si surface. Although there is no clear quantitative distinction between a weak and a strong chemical bond, we consider a species bounded with less than 1eV to be weakly bound. Thus, a lower limit of Si monomer activation energy is crudely estimated to be (4.56-1.0=)

3.56eV. The estimated range of the mobile Si monomer formation activation energy is then between 3.6-4.6eV. We note that this estimation overlaps with the measured range of the activation energy (3.5-4.3eV) of SiO formation[5]. On this basis, we expect that both SiO and Si monomer formation reactions can kinetically compete on the surface. Our STM studies described below confirm the above conclusion.

The experiment is conducted in an ultrahigh vacuum (UHV) system with base pressure <1 x 10-10 Torr. An ultrathin oxide (~ 10≈ thick from in-situ X-ray photoelectron spectroscopy measurements) is grown on an atomically clean Si(100) surface at 650∞C in 5 x 10-5 Torr O2 partial pressure. The oxide film is then annealed for different durations at 750∞C in UHV, and the resultant oxide surface morphologies are examined by STM after quenching the sample to room temperature. Figure 2 shows two STM images of the oxide film after annealing for 30 seconds and 90 seconds. It is apparent from the STM image sequence that the void number density increases with annealing duration in contrast to previous observations[2-4,6,7]. Also, before the void number density increases to the point that the voids start to coalesce, the void size increases and saturates[8].

These experimental observations are consistent with our theoretical calculations. The rate limiting step for void initiation is SiO formation, as it is the only process (reaction) involved in the void initiation. However, for the enlargement process, if Eact,SiO > Eact,monomer, one expects voids to enlarge at some rate without a substantial increase in void number density[1-4]. Alternatively, if Eact,monomer > Eact,SiO, one also expects void enlargement but at a substantially lower rate[6,7] accompanied by new void formation. Since we observe an increase in void number density concomitant with void enlargement in thermally grown ultrathin oxide films, our observation suggests that the activation energy of SiO formation and that of Si monomer formation must be comparable.

In conclusion, we have carried out combined theoretical and experimental studies to elucidate the the dominant reactions that control the oxide void growth. We estimate that the activation energy for a mobile Si monomer from Si(001)(2x1) dimerized surface is in the range of 3.6-4.6eV based on our GGA corrected density functional theory cluster model calculation. The calculated range of activation energy overlaps with the activation energy of SiO formation measured experimentally, suggesting that these two reaction mechanisms should kinetically compete on the surface. Our STM studies confirm this prediction where an increase of void and an increase in void number density are concomitant.

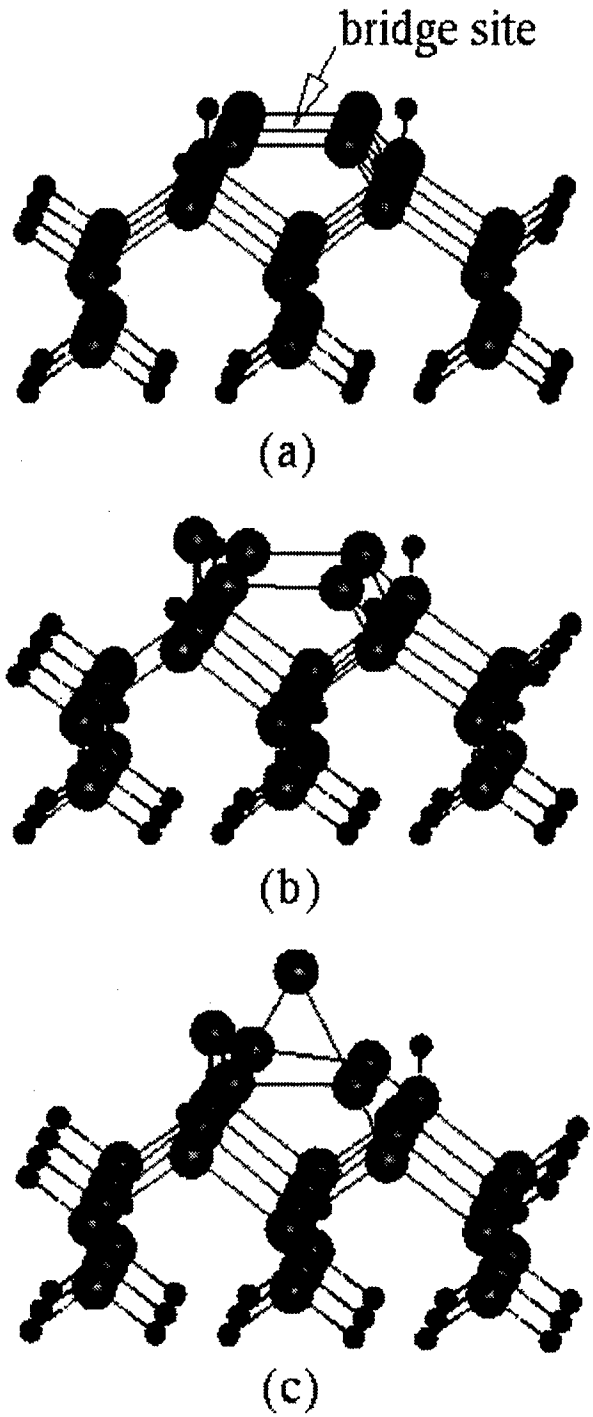

Figure 1. Three cluster models used in the calculation; Si and H atoms are represented by large and small solid circles, respectively: (a) Si35H36 cluster, Si(001)(2x1) dimerized surface; (b) Si34H36 cluster, Si(001)(2x1) surface with a vacancy; (c) Si35H36 cluster, monomer adsorption on bridge site near a vacancy

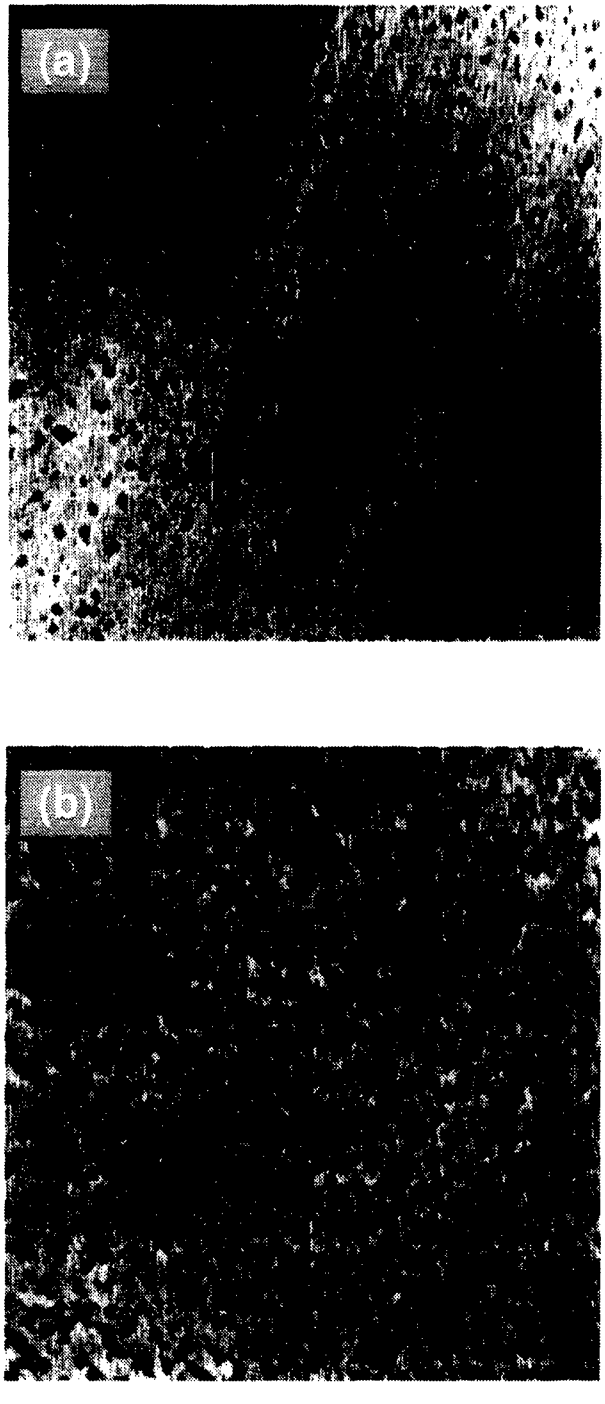

Figure 2. STM images acquired after annealing the ultrathin oxide film for (a) 30 seconds and (b) 90 seconds at 750 °C. Sample bias is +3 V.

Acknowledgment

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29. The adsorption energy for a monomer on the bridge site of an ideal Si(001)(2x1) surface is calculated to be 2.86eV. The small difference between the Si adatom adsorption energies on a surface with a vacancy and an ideal surface indicates that the presence of the vacancy only results in a local perturbation in the adsorption energy around the vacancy center.

Appendix F

Beyond-the-roadmap technology: Silicon heterojunctions, optoelectronics, and quantum devices (invited), *Materials Research Society Proceedings*, Boston, MA (1997).

Materials Research Society Proceedings, Boston, MA, December 3, 1997.

BEYOND-THE-ROADMAP TECHNOLOGY: SILICON HETEROJUNCTIONS, OPTOELECTRONICS, AND QUANTUM DEVICES

(Invited)

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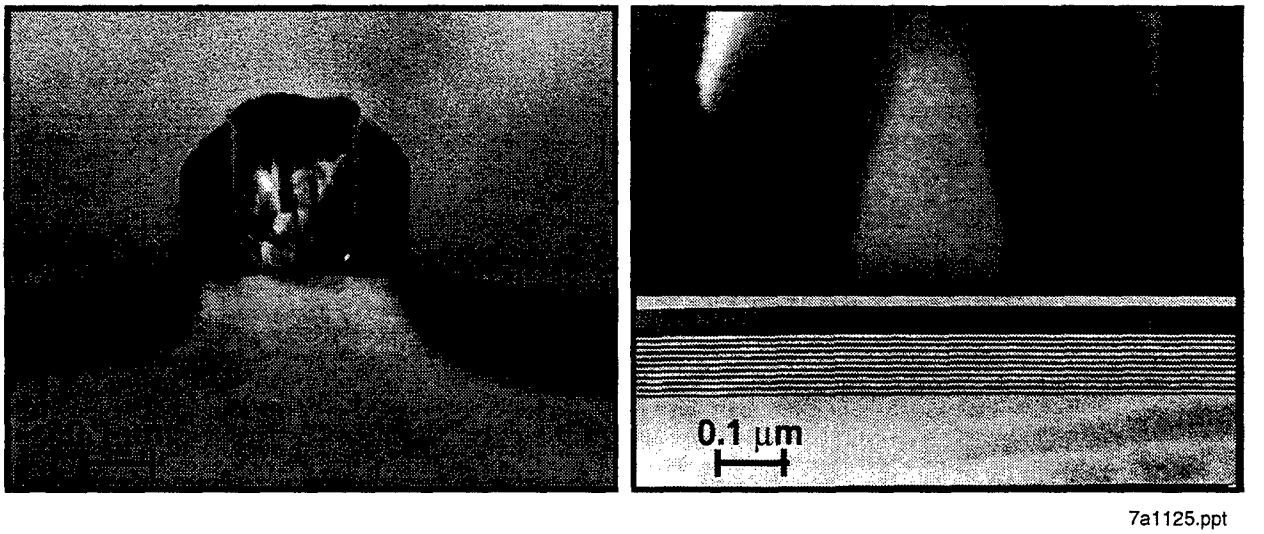
ABSTRACT

The roadmap for silicon device technology has been drawn, extending to the year 2010, and featuring a CMOS transistor with a gate length of 0.07 μm [1]. Beyond this point, silicon heterojunctions could provide a means to further device scaling. Silicon heterojunctions could also bring new devices to the silicon substrate including light emitters and detectors, and resonant tunneling diodes (RTDs). Today SiGe/Si and SiGeC/Si heterojunctions are receiving the greatest attention, but heterojunctions now being developed to realize silicon RTDs are increasing the heterojunction options for silicon-based quantum-well and optical devices. Here we outline the fundamental device requirements for silicon optical and tunneling devices and describe progress on silicon heterojunction development towards demonstration of silicon-based RTDs. Materials now under study include, ZnS, crystalline oxides and nitrides; new processes could provide methods for forming crystalline materials over amorphous barriers.

INTRODUCTION

Striking differences between high performance silicon and compound semiconductor device approaches can be seen in the cross-sectional micrographs of Figure 1. Shown at left is an 0.18 μm MOSFET (metal-oxide-semiconductor field-effect transistor) with a polysilicon gate and a gate oxide of approximately 5 nm. In the MOSFET, the energy band profiles in both the lateral and vertical directions are engineered by close control of the dopant profiles. The dark contrast in the transmission electron micrograph (TEM) of Figure 1(a) is caused by strain induced by the



(a) (b)

Figure 1. Comparison of (a) the silicon MOSFET and (b) the InP-based HFET at the same scale and contrasting the differences between dopant and bandgap engineering.

heavy source/drain implants. In contrast, Figure 1(b), an InP-based 0.2 μm gate heterojunction field-effect transistor (HFET) is shown at the same scale through a composite figure consisting of a scanning electron micrograph (SEM) of the gate above a TEM of the underlying epitaxy appropriately scaled. A silicon heterojunction technology which could harness both dopants and heterojunctions would enable a new flexibility in the optimization and continued scaling of MOS device technology.

Heterojunctions on silicon could also enable the construction of tunable silicon light emitters, detectors, optical interconnects, and tunneling devices. High performance resonant and interband tunneling diodes, when combined with any transistor technology allow circuit compaction which can provide a speed increase of 2 to 5× and a reduction in power dissipation by a similar factor. Circuit simulations and layouts of RTDs in a CMOS process have shown that static power dissipation can be reduced by approximately 100× in embedded memory/logic applications. For more information on resonant tunneling circuit technology consult references [2-4].

In this paper, we outline the materials requirements for silicon based heterojunction device development and review current progress in the development of silicon heterojunctions for RTDs. We find that the fundamental materials requirements for Si tunneling devices are the same as for photonic sources; this is easy to accept since the RTD is the first step in the fabrication of the silicon-based superlattices. In the experimental section, we outline recent progress in the development of amorphous, crystalline, and mixed amorphous/crystalline heterojunctions toward the demonstration of resonant tunneling diodes.

Relationship Between Optical and Tunneling Devices

For devices which are not small in cross section (greater than ~100 nm^2), there are two classes into which we can group both tunnel devices and optical devices such as sources and detectors. The two classes are (i) unipolar or intraband and (ii) bipolar or interband. The energy and momentum conservation laws which govern the performance of both tunnel devices and optical devices are the same for each class. For intraband devices in which the transport or absorption and emission takes place solely within either the conduction or valence band, both conservation of total energy and transverse momentum are required to obtain good performance. This is because in intraband devices, there are no energy gaps, only momentum gaps. For interband devices in which electrons tunnel or optically recombine across the bandgap, only conservation of total energy is required to obtain good performance. Thus, interband devices, either electrical or optical, tend to be more resilient to the effects of disorder since they require one less conservation law to work.

Figure 2(a) illustrates the energy and momentum conservation requirements of a unipolar RTD. The horizontal line in the well between the two barriers is generally referred to as the energy level of the resonant state in the well or the "resonant energy." However, it is actually the bottom of a 2-dimensional (2D) subband of states represented by a parabola. In Figure 2(a), the RTD is biased in the valley current region such that the electron in the emitter with zero transverse momentum is incident at an energy above the "resonant energy." In an ideal epitaxial structure, the periodic crystal potential is undisturbed in the transverse plane, therefore transverse crystal momentum is conserved, and the process illustrated in Figure 2(a) is not allowed. In the presence of disorder from, for example, impurities, alloy, or interface roughness, the incident electron can pick up a Fourier component of the disorder potential and scatter into a transverse momentum state k_t'. This is the process by which elastic scattering from disorder contributes to the valley current.

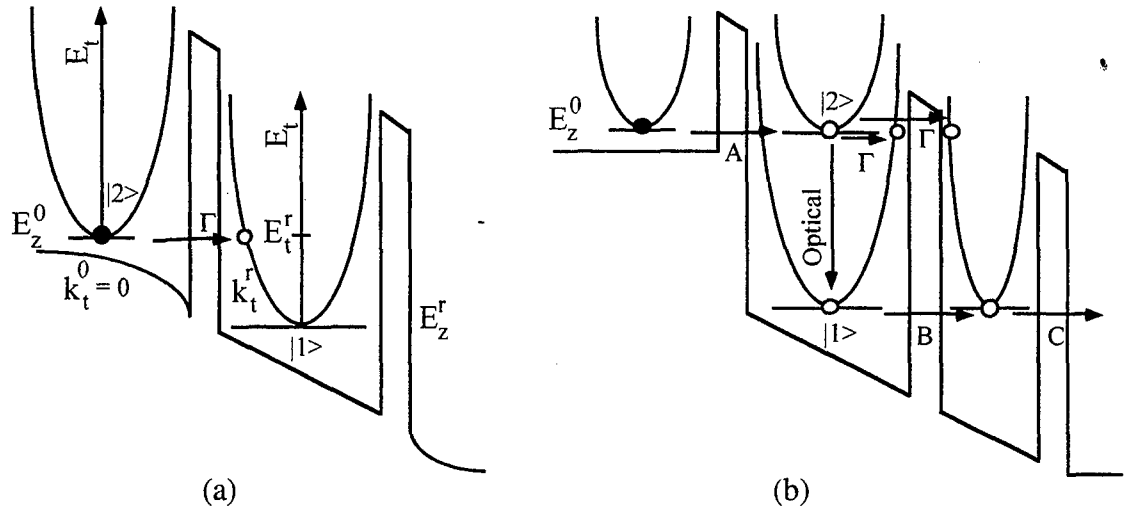


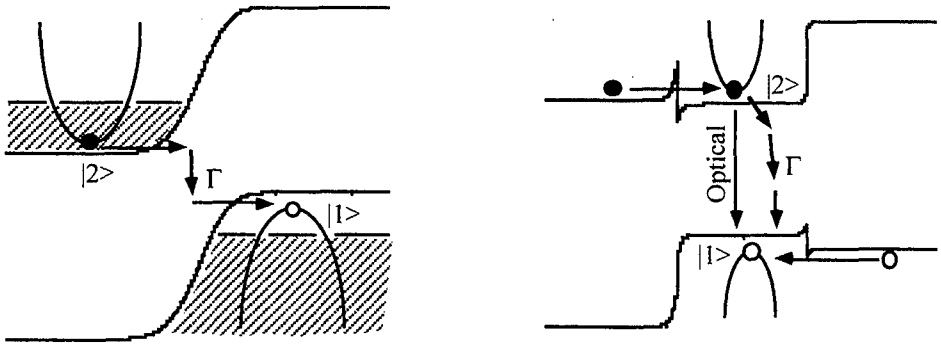
Figure 2. Comparison of unipolar intraband tunnel and optical devices: (a) resonant tunneling diode and (b) optical light emitter. The parabolas shown on the energy band diagrams represent the transverse kinetic energy. An off-resonant incident electron in (a) with longitudinal energy E_z^o and zero transverse kinetic energy cannot tunnel and conserve total energy and transverse kinetic energy. The processes labeled Γ can occur if transverse momentum is not conserved such as in amorphous materials; breaking transverse momentum conservation results in an increase in valley current in RTDs and a reduction in the quantum efficiency of optical devices.

Therefore, any process, either elastic or inelastic, that destroys transverse momentum conservation, reduces the peak-to-valley ratio (PVR) of a unipolar RTD.

In a similar way, lack of transverse momentum conservation reduces the performance of intraband optical devices which are based on electron transitions from one "resonant state" to another. A schematic example of an infrared source is shown in Figure 2(b). An electron is injected from the emitter into the second resonant state in the left well. Ideally, it will then optically recombine with the hole in the first resonant state and then tunnel out into the collector following the path A-Optical-B-C. However, if transverse momentum conservation is broken, the processes labeled Γ can also occur. These processes reduce the quantum efficiency of the device.

For interband tunnel diodes such as the Esaki diode [5], the quantum well Esaki diode [6], or the resonant interband tunnel diode [7], only conservation of total energy is required to obtain good performance since a true energy gap exists between the electron and hole states. Figure 3 compares the (a) Esaki diode biased into the valley current region with the (b) interband optical source. Neither device requires transverse momentum conservation to work. The tunneling event labeled Γ in Figure 3(a) is prohibited in an ideal Esaki diode by energy conservation. Only processes that destroy the energy conservation of the tunneling electron such as phonon or photon emission reduce the peak-to-valley current ratio and device performance. Therefore, interband tunnel devices should be more resilient to scattering due to disorder than intraband tunnel devices. This is evident for an Esaki diode since the active region is doped to concentrations of 10^{20} cm^{-3}; such a high doping in the well of an RTD would destroy its NDR.

In the same way, interband optical devices rely only on energy conservation for their operation. Figure 3(b) shows an interband optical source. Electrons are injected from the *n*-contact on the left into the well where they optically recombine with holes injected from the *p*-contact on the right. The quantum efficiency of this device is not effected if electrons do not conserve their transverse momentum. However, any nonradiative recombination reduces the efficiency of this device;



(a) (b)

Figure 3. Comparison of bipolar interband tunnel and optical devices: (a) Esaki diode biased into the valley current region and (b) optical light emitter. The Esaki diode and interband optical source do not require transverse momentum conservation.

nonradiative recombination requires an inelastic process for an electron to lose the energy of the bandgap.

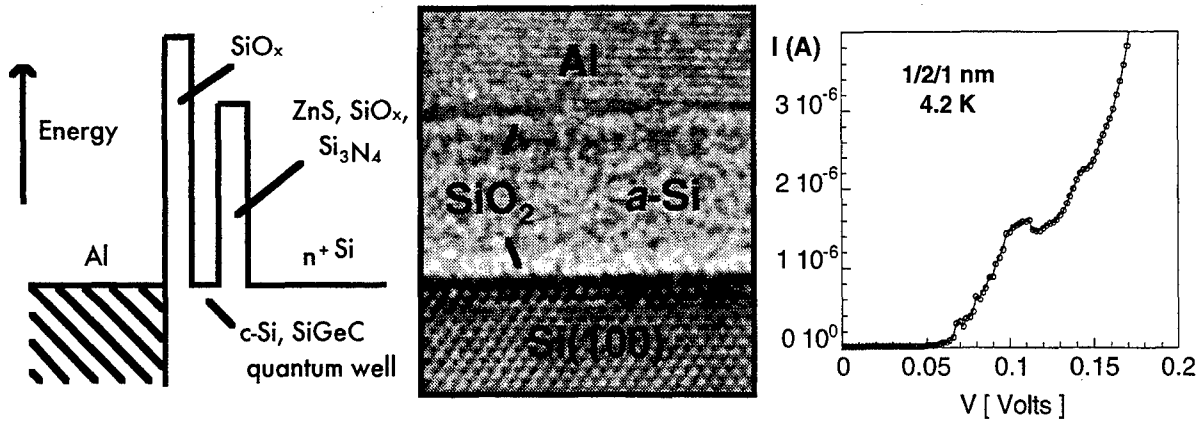
The performance of both tunnel devices and optical devices is limited by the nonradiative recombination from state |2> in subband 2 to state |1> in subband 1. This recombination process is labeled as the Γ process in Figures 2 and 3. The nonradiative recombination rate from subband 2 to 1 in intraband devices, Figure 2, is fast since the subbands are degenerate. The nonradiative lifetime resulting from phonon emission is on the order of 1 ps. For interband devices, the nonradiative lifetime is much longer. For an interband device, an electron must emit multiple phonons to lose an energy on the order of the bandgap and the recombination process is mediated by localized states in the bandgap. Nonradiative lifetimes of interband devices can be on the order of 1 ns resulting in a better quantum efficiency than intraband devices. The key point is that the performance of interband devices is not effected by momentum conservation, therefore interband devices should be more resilient to the presence of disorder.

EXPERIMENT

Amorphous Si/SiO_2 Superlattices and Resonant Tunneling Diodes

Experiment is consistent with the above theoretical discussion for both amorphous Si/SiO_2 superlattices and resonant tunneling diodes. There have been a number of studies of the optical properties of Si/SiO_2 superlattices to look for quantization and resonance effects [8,9]. Core level x-ray spectroscopy and photoluminescence gives strong evidence that quantization does occur, and that it follows the common inverse-square relationship to the well width [8]. The observation of state-quantization in these superlattices is to be expected despite the fact that the Si/SiO_2 superlattices are amorphous since the optical processes require only conservation of total energy.

In the case of resonant tunneling diodes formed out of the amorphous $SiO_2/Si/SiO_2$ double barrier there have been no high-PVR demonstrations of resonant tunneling and negative differential resistance (NDR). This is also consistent with theoretical expectations, since the observation of NDR requires conservation of both total energy and transverse momentum and transverse momentum is not conserved in amorphous materials. The random potential resulting from the amorphous Si/SiO_2 heterostructure breaks the translational periodicity and thus the transverse momentum conservation required for high PVR in RTDs. Typical findings for this system are illustrated in Figure 4.



(a) (b) (c)

Figure 4 Silicon resonant tunneling double barrier: (a) schematic energy band diagram, (b) transmission electron micrograph of an amorphous resonant tunneling heterostructure with oxide thicknesses of 0.9 nm and quantum well width of 2 nm, and (c) measured current-voltage characteristics of an amorphous RTD like the device pictured in (b) at low temperature showing negative differential resistance (150 μm device diameter). The peak-to-valley current ratio is low and the characteristic varies widely from device to device; The peak voltage does not scale inversely as the square of the quantum well width. The negative differential resistance at 1.1 V is probably associated with zero-dimensional states (due to dangling bonds, interface or impurity states, or defects) located within the double barrier.

The amorphous SiO_2 barriers shown in Figure 4(b) were grown by a room temperature ultraviolet (UV) ozone process, but similar results are also obtained for oxides grown by thermal dry oxidation. The amorphous Si quantum well was deposited at room temperature in an MBE (molecular beam epitaxy) chamber. The aluminum top contact which serves as the positive terminal or collector of the RTD is typically formed *in situ* before removal from an ultrahigh vacuum system which allows oxidation, MBE, and metallization processes without breaking vacuum.

Numerical simulations of the current-voltage (I-V) characteristics for amorphous devices has shed some light on the experimental RTD results [10]. Current-voltage calculations that include scattering in the amorphous material as a random potential show clearly that the resonance width is directly related to the strength of the scattering as shown in Figure 5. Carrier mobility in the material is shown to be a useful parameter for characterizing the scattering in the amorphous structure. *The essence of the theoretical analysis is that crystalline material, at least in the well region, is necessary to observe resonant tunneling in these materials.* Simply speaking the lack of crystalline periodicity results in increased carrier scattering thereby causing the resonances in the structure to broaden. The broad resonances manifest themselves in poor or non-existent peak-to-valley ratios for resonant-tunneling diodes. However, one important additional conclusion from the theoretical analysis is that scattering sites in the *barriers* do not significantly effect the electron transport because of the (exponentially) reduced amplitude of the electron wavefunction within the barrier. This has motivated the fabrication approach which follows.

Formation of Crystalline Silicon on Ultrathin Voided Oxides

The barriers used in a resonant tunneling diode or superlattice can in principle be porous i.e. the barrier such as SiO_2 can have nanometer sized voids through which a silicon overlayer can be

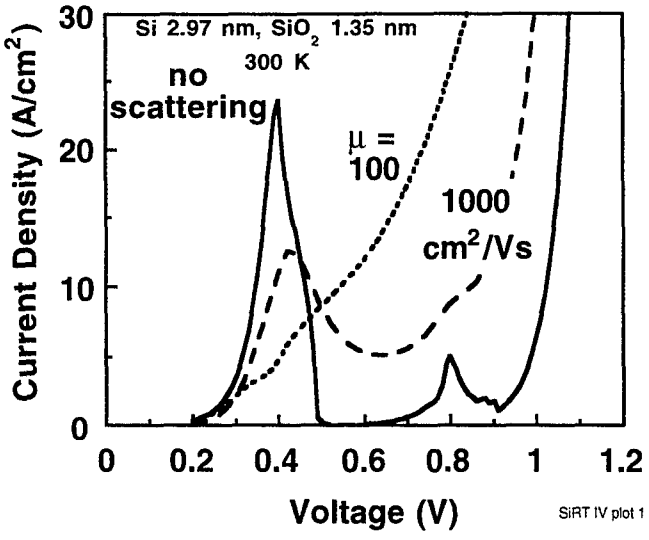


Figure 5. Computed current-density voltage charactistic showing the improvement of peak-to-valley current ratio with electron mobility (crystallinity) in the quantum well where a random potential proportional to the carrier mobility is used to explore the effects of scattering in the amorphous heterostructure [10].

nucleated. If the voids in the tunneling barrier have openings of size smaller than the electron wave packet spread, the tunneling barrier height is not reduced and the nucleated Si quantum is crystallographically aligned to the underlying silicon. A method for forming these voids in ultrathin layers has been developed [11,12] using the thermal desorption of SiO at elevated temperatures in ultrahigh vacuum to form the voids, see Figure 6. In practice, as detailed in [11,12], we have found that there is a direct relationship between the size of the voids and their density, and that crystalline Si overgrowth on Si (100) is only obtained for large void densities (exceeding approximately 2500/μm^2) and large void area (exceeding approximately 400 nm^2). This void area is approximately one hundred times too large for practical growth of voided-barrier resonant tunneling diodes and optical sources.

Since the work of references [11] and [12] void formation and growth experiments in ultrathin thermal oxides on the Si (111) surface have been conducted and shown to exhibit similar behavior to that observed on Si (100). These results are summarized in Figure 7 where an increase in void

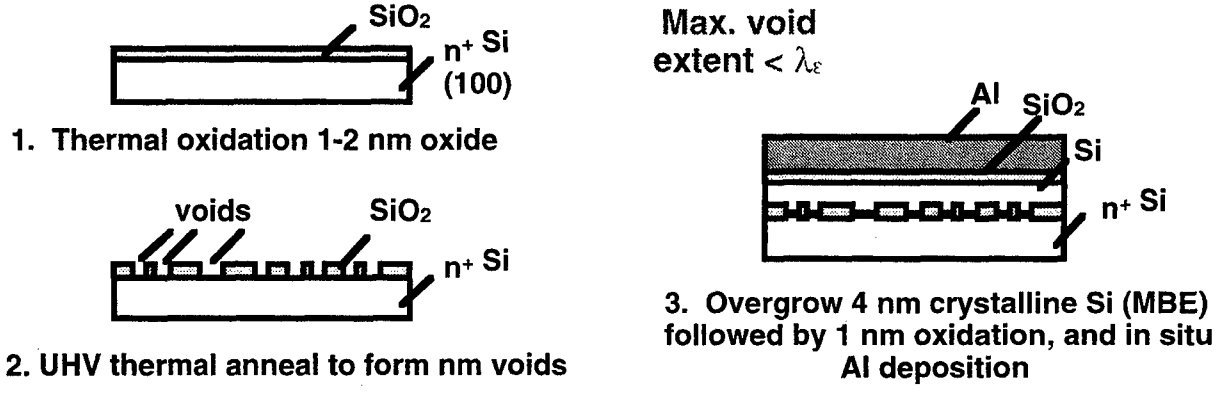


Figure 6. Schematic cross section of a process by which crystalline silicon is nucleated through a voided amorphous barrier.

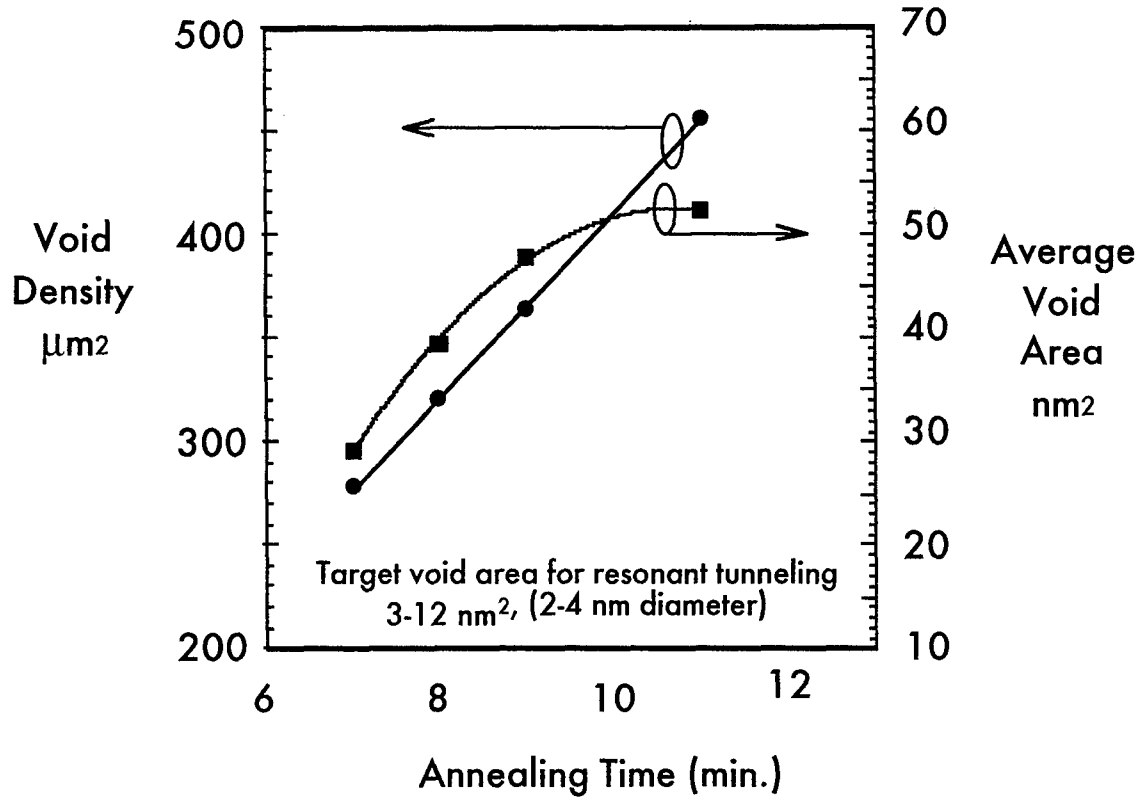


Figure 7. Dependence of the density and area of voids formed in a 1 nm SiO_2 film on (111) Si on annealing in vacuum at 750 °C for the indicated times. Void area and density is determined by scanning electron microscopy.

density and size are again observed with anneal time. Interestingly, the formation of observable voids requires a longer period of time at temperature, suggesting that the void initiation on the (111) surface is more difficult than on the (100) surface. Like the (100) surface, the smallest oxide void areas found on the (111) surface (~29 nm^2) do not meet the targets (3-12 nm^2) for use in oxide/silicon/oxide RTDs.

Formation of Crystalline Silicon on Amorphous Barriers by Lateral Overgrowth on SiO_2 Islands

A second method now under investigation for resonant tunneling diodes using $SiO_2/Si/SiO_2$ double barriers is illustrated in Figure 7. In this case, the crystalline Si quantum well is formed over lithographically-defined oxide islands, by molecular beam lateral epitaxial overgrowth. The greater silicon surface provides the seed for lateral crystalline overgrowth of the oxide islands. Since the silicon overgrowth process is formed on a micron-scale to submicron scale and the RTD emitter contacts are as small as 0.01 square microns, the current through a single RTD can easily become less than 10 fA if the oxide thicknesses become large (>2 nm). For this reason arrays of RTDs are formed in addition to the single device: array sizes of 10, 100, 1000, and 10,000 RTDs allow parallel measurements of the average current through an RTD when the single device current is too low to be easily measured individually. The most critical steps are those which lead to step 1. To begin, a thermal oxide of about 4 nm is grown on an HF terminated Si (100) surface. Submicron islands are then formed by photolithography and the oxide mesas are formed by wet etching in buffered HF. Just prior to loading for growth of the quantum well, the 4 nm oxide is

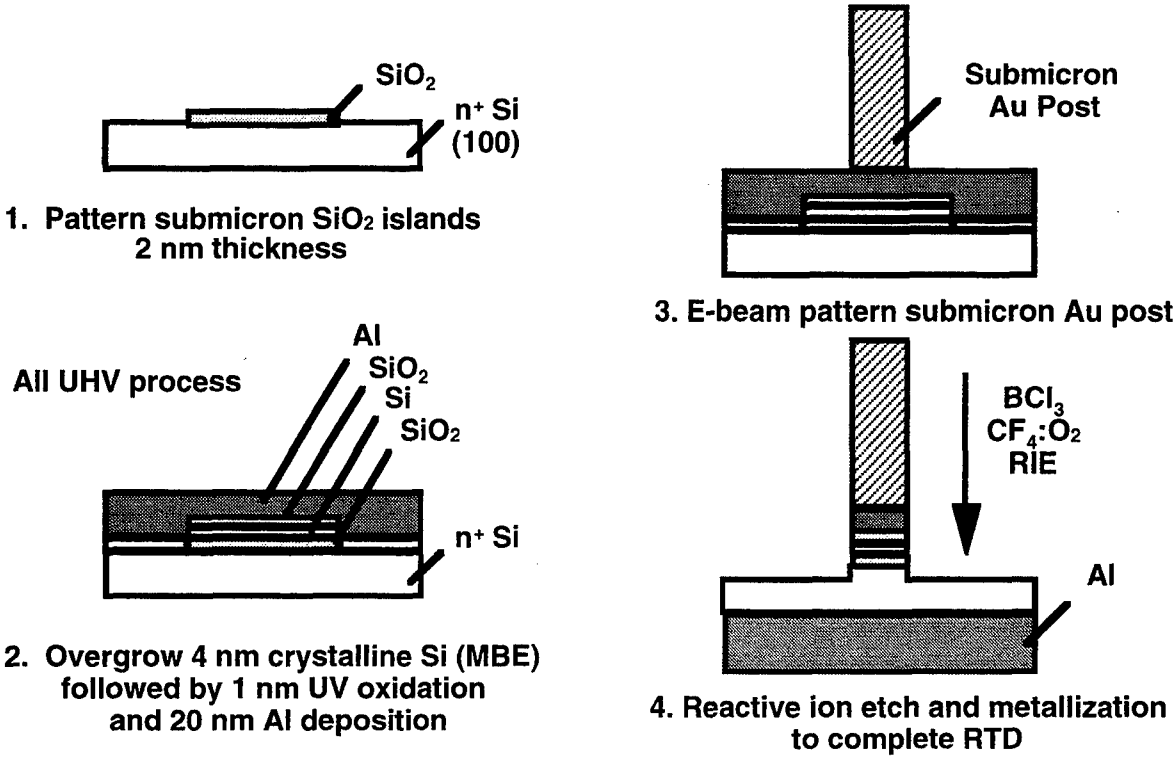


Figure 8. Schematic diagram of a process under development for realization of resonant tunneling diodes with amorphous Si barriers and crystalline Si quantum well.

thinned by wet chemical etching again in buffered HF to thin the oxide below 2 nm and hydrogen terminate the greater Si surface for growth. Scanning electron micrographs of the overgrown oxide/silicon/oxide double barrier are shown in Figure 9. This image is taken after the emitters have been deposited and before reactive ion etching to form the active device areas; it is also taken

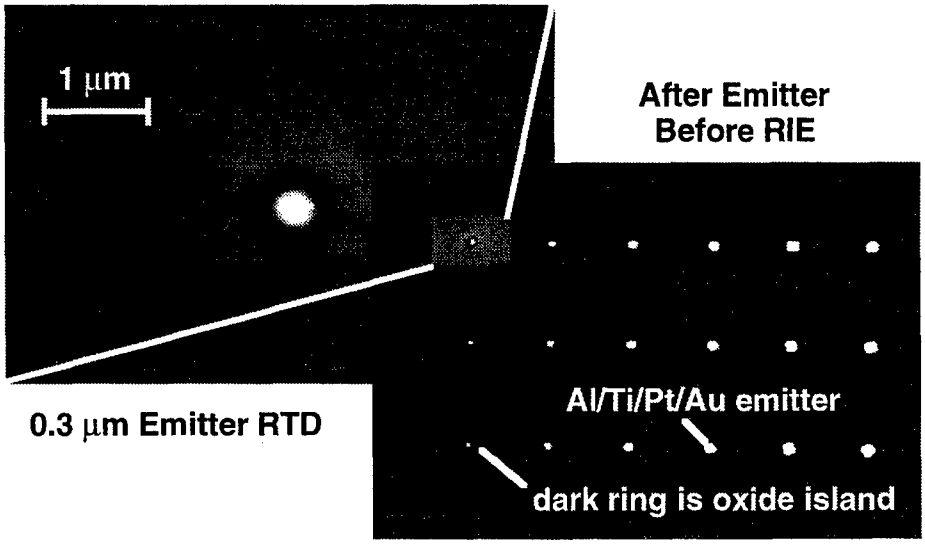


Figure 9. Scanning electron micrographs of the $SiO_2/Si/SiO_2$ resonant tunneling diode (wafer A4) taken after emitter formation over the double barrier. The first oxide islands are seen as dark regions about the submicron emitters.

from a region of the wafer from which the *in situ* deposited aluminum has been masked away. What can be seen in the lower right micrograph are 18 different RTD emitters, the first row with 0 degree orientation, the second row with a 15 degree rotation, and the third row with a 30 degree rotation. About each emitter a dark ring is seen corresponding to the location of the first and underlying oxide island. The expanded region in the upper left was taken first and the charging of the second surface oxide is apparent in the second, lower right figure where the charged surface has more emission than the previously uncharged surface. This is qualitative confirmation of the presence of the second oxide.

Crystalline Silicon Heterojunctions

Silicon heterojunction research has recently focused on the SiGe/Si and SiGeC/Si systems which should provide conduction band offsets as high as approximately 0.5 eV in the limit of high Ge content where only thin layers can be grown without lattice relaxation. Silicon germanium and its alloys with carbon [13] do not provide the broad bandgap flexibility enjoyed by the compound semiconductor systems. The SiO_2/Si heterostructure with a band offset of 3.2 eV provides an excellent barrier for use as a gate oxide and when formed at thickness below approximately 4 nm provides textbook direct tunneling barrier [14], but bandgap engineering are difficult due to it's lack of crystallinity and the difficulty with silicon overgrowth.

A single crystal silicon oxide would provide several opportunities for advanced device development. First and foremost, given a crystalline silicon oxide barrier, it should then be possible to grow single crystal Si over the insulating oxide. We have developed a method for growing a single crystal silicon oxide layer directly on a Si (100) substrate, which is not fully SiO_2, but rather is a suboxide SiO_x ($0 < x < 2$) which is still insulating and could serve as the insulating barrier while still provide an epitaxial template for subsequent overgrowth of a crystalline Si quantum well. Crystalline SiO_x films (200 nm thick) have now been demonstrated, with oxygen contents ranging from 20 - 40%, as determined by Rutherford backscattering (RBS) measurements. The crystal quality of the top Si layer has also been measured by RBS, and although it is defective (several films had $c_{min} = 20\%$, where $c_{min} = 3\%$ for a perfect epitaxial Si film). Single-barrier tunnel diodes have been constructed and show that the desired insulating property of the barrier is maintained with a barrier height of approximately 0.5 eV.

The need for crystalline insulating layers on Si which can be used as seeds for crystalline Si overgrowth has motivated us to consider the growth of crystalline silicon nitride. We have now demonstrated growth of an ultrathin crystalline nitride on a Si (111) substrate. The crystalline layer was grown by thermal nitridation in an NH_3 ambient, at a partial pressure of 1×10^{-5} Torr. In order to obtain growth of a crystalline nitride, the substrate must be heated above the 1 x 1 to 7 x 7 transition on Si (111), which occurs at 840 °C. Above this temperature, an 8/3 x 8/3 reconstruction is obtained, as shown in the 36 nm x 36 nm scanning tunneling micrograph in Figure 10. This crystalline insulator could provide an epitaxial template for subsequent overgrowth of a crystalline Si quantum well. Although the lattice mismatch between Si_3N_4 and Si is large (~20%), this reconstruction corresponds to a stoichiometry of Si_3N_5.

The crystalline oxides and nitrides offer one path to forming an epitaxial template for overgrowth of crystalline silicon. With an energy gap of 3.6 eV and a lattice constant of 5.42 Å, zinc sulfide (ZnS) is an excellent candidate for use as an insulating barrier that is lattice-matched to silicon. Recently, high quality ZnS layers on silicon have been realized by initiating MBE growth on a vicinal Si (001) surface (4° off-cut towards the $[0\bar{1}1]$direction) that has been terminated with

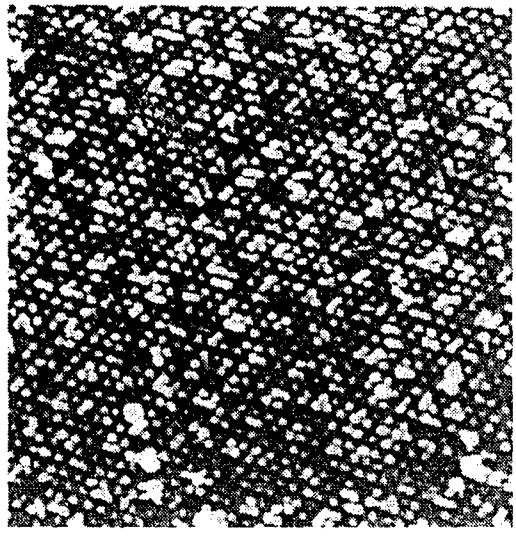


Figure 10. Scanning tunneling micrograph showing an 8/3 x 8/3 reconstruction of an epitaxial silicon nitride film grown on a Si (111) substrate.

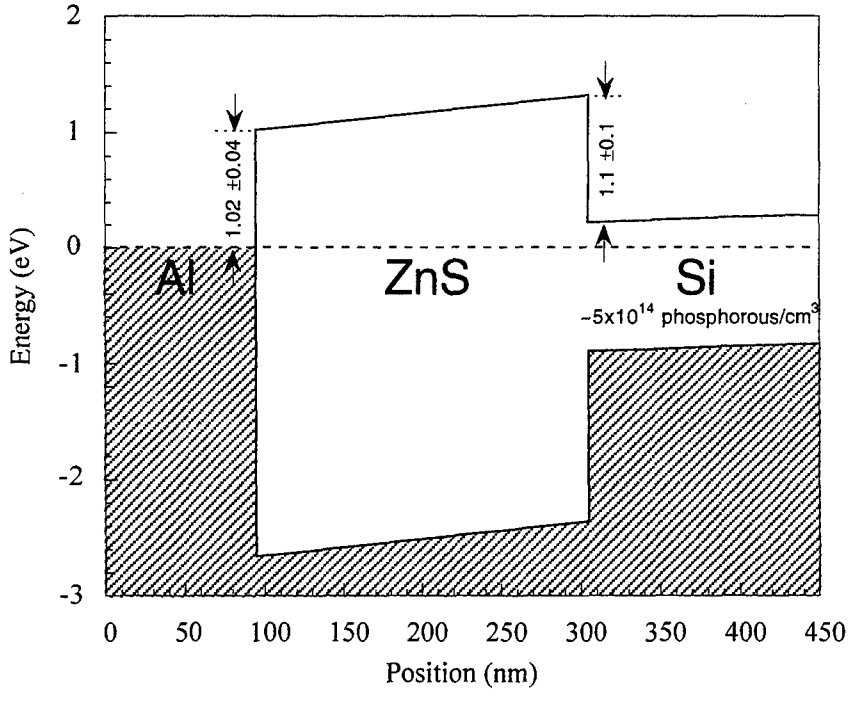


Figure 11. Zero-bias energy band diagram for Al/ZnS/As(1ML)/Si structure.

a single monolayer (ML) of As [15,16]. The band offsets for this heterojunction have also been determined [17]. Figure 11 shows the energy band diagram for the Al/ZnS/As(1ML)/n-Si heterostructure. The approximately 1 eV ZnS barrier heights to Al and Si, being much larger than kT at room temperature, are encouraging for the future room-temperature operation of ZnS/Si RTDs and superlattices.

CONCLUSIONS

We have shown that the energy conservation requirements for tunneling and superlattice devices are the same and that amorphous barriers should be acceptable for superlattice optoelectronic and resonant tunneling devices, so long as crystalline Si overlayers can be overgrown with crystalline registry to the underlying silicon substrate. Towards this end we have described two processes now under development to form resonant tunneling diodes using amorphous silicon dioxide tunnel barriers.

Silicon heterojunction growth is still in its early stages of exploration. Among the most promising new junction materials for Si are crystalline oxides, crystalline nitrides, and II-VI compounds such as ZnS. Other materials such as aluminum nitride, cerium oxide, and gallium phosphide deserve attention.

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